A 1.5 nW, 32.768 kHz XTAL Oscillator Operational From a 0.3 V Supply

Aatmesh Shrivastava, Divya A. Kamakshi, and Benton H. Calhoun

***Abstract*—This paper presents an ultra-low power crystal (XTAL) oscillator circuit for generating a 32.768 kHz clock source for real-time clock generation. An inverting amplifier operational from 0.3 V V_{DD} oscillates the XTAL resonator and achieves a power consumption of 2.1 nW. A duty-cycling technique powers down the XTAL amplifier without losing the oscillation and reduces the power consumption to 1.5 nW. The proposed circuit is implemented in 130 nm CMOS with an area of 0.0625 mm^2 and achieves a temperature stability of 1.85 ppm/°C.**

***Index Terms*—32 kHz XO, clock source, crystal (XTAL) oscillator, Internet of Things (IoT), real-time clock (RTC), subthreshold, ultra-low power (ULP).**

I. Introduction

ULTRA-LOW power (ULP) systems such as wireless sensor nodes (WSNs) for emerging Internet of Things (IoT) applications spend a large portion of their time in inactive or idle mode to save power. A typical operation of a ULP system constitutes a short burst of activity followed by a long idle time. The short burst of activity consumes higher power, whereas the power consumption in idle mode is relatively small. Spending a large time in the idle mode saves energy and can help with recharging the storage capacitor of energy harvesting ULP systems [1] from low energy ambient harvesting sources. To maximize idle time while remaining functional in a larger interconnected IoT network, these systems require precise clock to synchronize and wake-up the system at regular intervals. A real-time clock (RTC) utilizing an ULP oscillator is often used for this purpose. The total power consumption of such a system may be determined by the power consumption of the RTC. To reduce the power consumption and to increase the life-time of the system, the power consumption of the RTC needs to be reduced. In this paper, we present a 32.768 kHz crystal (XTAL) oscillator for RTC applications with a power consumption of 1.5 nW.

Widely varied circuit architectures ranging from on-chip oscillators to off-chip XTAL oscillators exist for the implementation of the RTC in an ULP system. A precision CMOS relaxation oscillator is presented in [2]. It achieves a temperature stability of 60 ppm/°C, but its power consumption is 45 μW for a 14 MHz clock. Further, the oscillator shows a power supply variation of 16 ppm/mV. A 150 nW, 100 kHz on-chip oscillator achieves a temperature stability of 5 ppm/°C for a temperature range of 20 °C–40 °C and 14 ppm/°C for a temperature range of 20 °C–70 °C [3]. The power supply variation of this oscillator is 0.1%/mV. The temperature stability and the power consumption of the oscillator make it suitable for ULP applications, but it requires a very controlled power supply. On-chip oscillators, using the gate leakage current, have been proposed in [4]–[6]. These designs employ calibration for temperature compensation and achieve a best temperature stability of 32 ppm/°C. The power supply variation of this oscillator is 0.42%/mV. Further, these oscillators can operate only at very low frequency (0.1–10 Hz) due to the low magnitude of gate-leakage current. The lower output frequency and higher power supply variation limits their usage for precise RTC applications.

A XTAL oscillator provides a very precise output frequency ($\sim 5-20$ ppm/°C) that is not affected by process or power supply variation by using an off-chip electro-mechanical XTAL resonator. Although off-chip components can increase the cost and volume of the system, XTALs are now being explored for ULP systems that require precise timing for wake-up or synchronization of a WSN in an IoT network. The power consumption of the XTAL used in ULP systems must be very small. Recent work on the design of 32 kHz XTAL oscillators show power consumption in the single digit nW range [7], [10], making it possible to use them for ULP applications. Power consumption of XTAL oscillators can be reduced by lowering the amplitude of oscillation by operating at lower voltages. Low power electronic watches use this technique to operate XTAL oscillator circuits in the subthreshold or weak inversion region of operation of the transistors [8]. The XTAL oscillator circuit proposed in [9] achieves a power consumption of 22 nW operating with a power supply (V_{DD}) around 600 mV. A delay locked loop (DLL)-based XTAL [10] achieves a power consumption of 5.58 nW. It also achieves lower swing to reduce the power consumption in the XTAL's effective series resistance (ESR). However, to reduce the power consumption and to maintain low swing for oscillation, it needs two power supplies and two grounds. It also requires a large area for its implementation. A self-charging XTAL design reduces the power consumption to 1.89 nW [7]. In this circuit, XI and XO are operated in a self-charging loop, where both XI and XO are charged based on the operating phase of the oscillator using only the parasitic load capacitors. In conventional designs, the input of the oscillator XI is obtained from XO as a filtered output through

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the high quality XTAL. The spectrum of XI will contain only the resonance frequency of the oscillator. However, the self-charging scheme [7] charges XI too to maintain the oscillation. The circuit used for charging XI can introduce additional frequency components in XI, which may degrade the spectrum of the oscillator.

In this work, we present a 1.5 nW, 32 kHz XTAL oscillator, which operates the XTAL with a feedback amplifier operating at 300 mV. We propose a technique of duty cycling the XTAL oscillator in conjunction with operating them in a subthreshold region. We achieve a measured average power consumption of 1.5 nW across 25 chips. In Section II, we present the operation of the XTAL. Section III presents the low power amplifier design and Section IV presents the duty-cycling technique. Section V presents measurement results.

II. XTAL Operation

An XTAL is an electromechanical resonator that resonates at its natural frequency when excited with electrical energy. Fig. 1(a) shows a conventional XTAL oscillator circuit. The equivalent circuit of an XTAL consists of a series RLC circuit with a parasitic parallel capacitor C_p. The frequency of oscillation is mainly determined by the motional inductor L_m and capacitor C_m. The ESR is the energy dissipating component of the XTAL. The inverting amplifier provides the negative resistance that overcomes the loss from ESR and pumps energy into the XTAL, making it oscillate at its natural frequency. The output frequency of the XTAL oscillator is very precise, and its stability is usually specified at parts per million or per billion (ppm/ppb). The extremely precise output frequency of XTAL oscillators makes them a natural choice for implementing clocks. Further, the frequency of oscillation is largely independent of voltage and process variation.

A. Theoretical Analysis for Low-Power XTAL Oscillation

The XTAL circuit can be made to oscillate in series or parallel mode. Parallel mode is the commonly employed mode of oscillation. In parallel mode, the XTAL is connected with an inverting amplifier with two load capacitors connected in parallel (C_L), as shown in Fig. 1(a). In parallel mode, the XTAL appears as an inductor and oscillates with the load capacitors (C_L). In order to oscillate, the circuit needs to meet the Barkhausen or the negative resistance criteria of oscillation. For negative resistance oscillation criteria, the amplifier needs to present a negative resistance ($R_{\rm NEG}$) at resonant frequency, whose absolute value should be greater than the XTAL's ESR ($R_{\rm ESR}$) [11] ($|R_{\rm NEG}| > R_{\rm ESR}$). We derive a theoretical analysis for a low power XTAL oscillator from the work presented in [8]. Fig. 1(b) shows a hypothetical three point oscillator. The negative resistance of the oscillator can be derived from [8, eq. (16)] as follows:

$$R_{\rm NEG} = \frac{-g_m C_L^2}{(g_m C_P)^2 + \omega^2 (C_L^2 + 2C_P C_L)^2}$$
$$R_{\rm NEG} = \frac{-g_m}{(g_m C_P/C_L)^2 + \omega^2 (C_L + 2C_P)^2}. \quad (1)$$

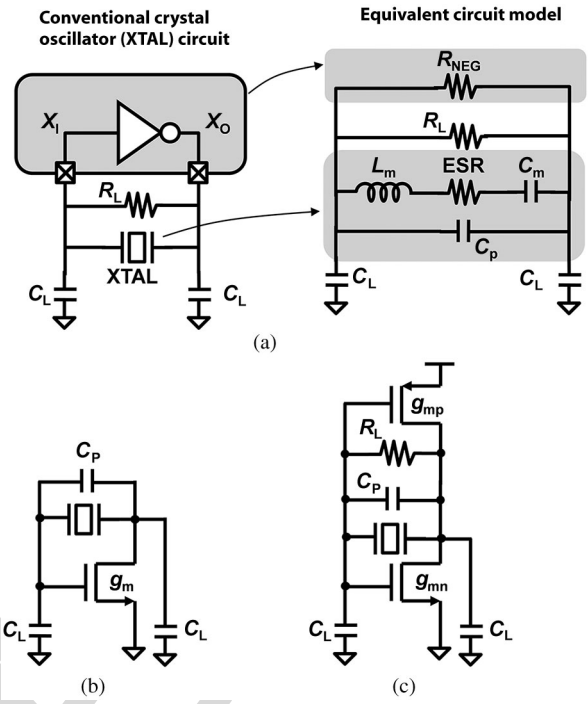


Fig. 1. (a) Conventional XTAL oscillator circuit and its equivalent representation. (b) Analysis of a three-point oscillator. (c) Practical implementation of XTAL oscillator with an inverter (push–pull oscillator). F1:1 F1:2 F1:3

Since $(g_m C_P/C_L)^2 \ll \omega^2 (C_L + 2C_P)^2$

$$R_{\rm NEG} = \frac{-g_m}{\omega^2 (C_L + 2C_P)^2}. \quad (2)$$

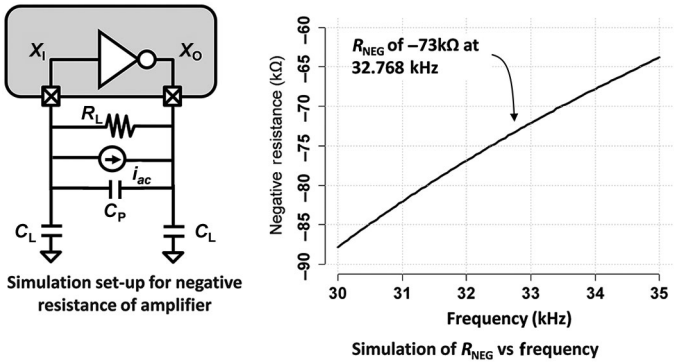
For an inverter-based oscillator, as shown in Fig. 1(c), the transconductance of both n*MOS* and p*MOS* devices will add, and the $R_{\rm NEG}$ can be approximately written as

$$R_{\rm NEG} = \frac{(-g_{mn} - g_{mp})}{\omega^2 (C_L + 2C_P)^2}. \quad (3)$$

For a device operating in subthreshold, the transconductance is given by

$$g_m = \frac{I_D}{nV_t} \quad (4)$$

where I_D is the drain source saturation current, n is the subthreshold slope approximately equal to 1.2, and V_t is the thermal voltage, which is 26 mV at room temperature. An n*MOS* biased at 7 nA of $\rm I_D$ gives a g_m of $2.24 \times 10^{-7} \Omega^{-1}$. Using the same value for g_{mn} and g_{mp}, (3) gives an $R_{\rm NEG}$ of -180 kΩ for a C_L of 6 pF and C_P of 1 pF. A power limit can be derived from (3) and (4) for various conditions. Assuming that a -60 kΩ $R_{\rm NEG}$ is sufficient for oscillation for a 30 kΩ ESR XTAL, an inverter running at 0.3 V can realize oscillation at 0.7 nW for a C_L of 6 pF. If a lower C_L value of 3 pF is used, then it is possible to achieve oscillation at 0.28 nW. Further, if one can realize an oscillator circuit at 150 mV V_{DD} as used in [7], then the power required to achieve oscillation is 140 pW with



F2:1 Fig. 2. Design method for the XTAL oscillator circuit.

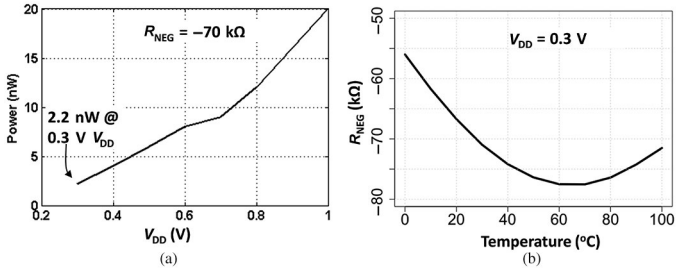


Fig. 3. (a) Simulation of XTAL oscillator power consumption across V_{DD} F3:1
with a fixed negative resistance of amplifier at -70 kΩ. (b) Simulation of F3:2
negative resistance of the amplifier with temperature at 0.3 V V_{DD}. F3:3

margin. In order to just barely meet the oscillation criteria, the power required sits at 70 pW.

B. Practical Design of a Low-Power XTAL Oscillator

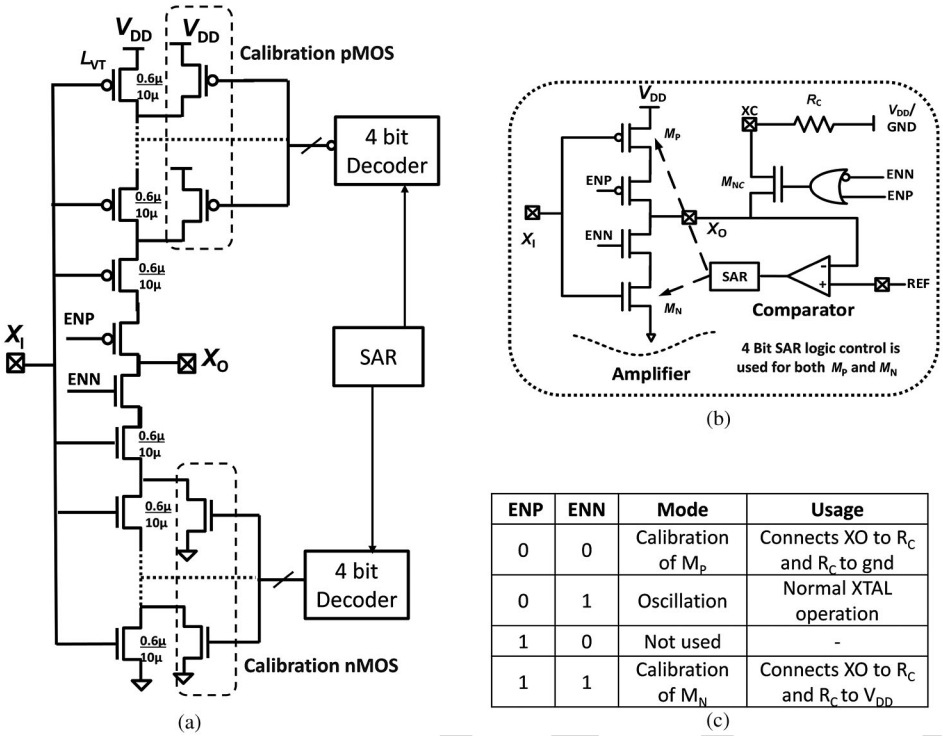
The preceding section showed the theoretical power required to achieve oscillation. However, several practical issues can reduce the $R_{\rm NEG}$ at subthreshold current levels. In this section, we present the practical design method for realizing the required $R_{\rm NEG}$ for oscillation, and Fig. 2 shows the design method. In this circuit, XTAL is removed from the oscillator, and an *ac* current source is connected across the amplifier terminal. The inverting amplifier presents an impedance to the applied ac current, which will have a real component at the oscillation frequency. The real component is the negative resistance ($R_{\rm NEG}$) of the amplifier at resonance. The value of $R_{\rm NEG}$ is a function of frequency. Fig. 2 shows the simulation of the $R_{\rm NEG}$ of the amplifier across frequency for a C_L of 6 pF and a C_P of 1 pF. The ESR of the XTAL oscillator at 32.768 kHz is typically in the range of 30 kΩ. The g_{mn} and g_{mp} of our oscillator is $1.12 \times 10^{-7}\Omega^{-1}$ and $1.16 \times 10^{-7}\Omega^{-1}$, respectively, at a bias current of 7 nA and V_{DD} of 0.3 V. Plugging these values in (3) yields a $R_{\rm NEG}$ of -90 kΩ. However, Fig. 2 shows that we can achieve a $R_{\rm NEG}$ of -73 kΩ. Further, the start-up time of the XTAL oscillator is in the range of $\sim$1 s because of the high quality factor (Q) of the XTAL resonator. The $R_{\rm NEG}$ of the amplifier also controls the start-up time, and a negative resistance with higher magnitude will reduce the start-up time of the XTAL [12].

The power consumption of the XTAL oscillator is determined by the XTAL and the amplifier. XTAL's ESR dissipates energy in the form of heat loss, as Joule's heating, which depends on the amplitude of oscillation. To reduce the power consumption of the XTAL oscillator, the amplitude of oscillation is often reduced. This can be done by operating the amplifier in the subthreshold region [8], [9]. In this paper, we propose a 32 kHz XTAL oscillator circuit that consumes 1.5 nW of power. We first operate the XTAL oscillator in subthreshold at 0.3 V V_{DD} to reduce the power consumption to 2.2 nW. We further reduce the power by applying a duty-cycling technique to turn-off the amplifier often. This technique brings down the over-all power consumption of the XTAL oscillator to 1.5 nW, improving the state-of-the-art by over 26%.

III. Low Power Amplifier Design

In this section, we present the design of the low power amplifier circuit. Various inverting amplifier architectures can be used to implement the amplifier. A simple push-pull inverter with a large bias resistor, as shown in Fig. 1, is one of the design options and is commonly used because it is single stage and hence consumes least amount of power [9]. However, the inverter circuit needs to be designed properly to meet the oscillation criterion. At lower drive strength (smaller sizes for *n*MOS and *p*MOS), the $R_{\rm NEG}$ of the amplifier is low and cannot meet the oscillation criterion. Increasing the size increases the $R_{\rm NEG}$. After a certain size, the $R_{\rm NEG}$ starts decreasing again because of the self-loading in the inverter through the gate-drain capacitance, C_{GD} (Miller-effect). Also, increasing the size of the inverter increases the power consumption. Therefore, the inverter needs to be sized properly for the power consumption, as well as for $R_{\rm NEG}$. Further, the power consumption can also be reduced by operating the amplifier circuit at a lower V_{DD}. At lower V_{DD}, the amplifier device sizes are typically bigger than the sizes for higher V_{DD}. However, the overall power consumption decreases. Fig. 3(a) shows the power consumption of the amplifier circuit designed to provide a fixed negative resistance of -70 kΩ at 32 kHz for different $V_{DD}s$ with a C_L of 6 pF and C_P of 1 pF. The power consumption increases with the voltage almost linearly. This is largely because the bias current of the amplifier almost remains the same for a given $R_{\rm NEG}$, which can be confirmed by inspecting equations (3) and (4). As a result, power increases because of the increase in the V_{DD}. Therefore, the oscillator needs to be operated at a lower V_{DD} to reduce the power. Further, the g_m of the amplifier is a weak function of temperature, so the $R_{\rm NEG}$ does not vary a lot with temperature as shown in Fig. 3(b). Our amplifier consumes 5–10 nA of quiescent current during start-up, which decreases after the saturation of oscillation. The power consumption of the XTAL oscillator is 2–10 nW at 0.3 V V_{DD}.

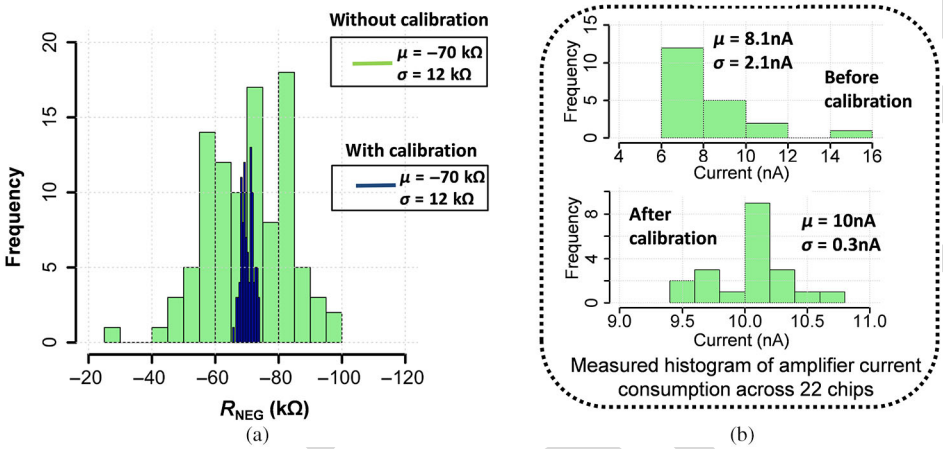
Fig. 4(a) shows the circuit diagram of the proposed amplifier. We use low threshold ($L_{\rm VT}$) transistors with longer length to implement the amplifier. $L_{\rm VT}$ transistors give better performance at 0.3 V V_{DD}, owing to the lower threshold voltage, while a longer length of the transistor helps in reducing the



ENP	ENN	Mode	Usage
0	0	Calibration of M_P	Connects XO to R_C and R_C to gnd
0	1	Oscillation	Normal XTAL operation
1	0	Not used	-
1	1	Calibration of M_N	Connects XO to R_C and R_C to V_{DD}

(c)

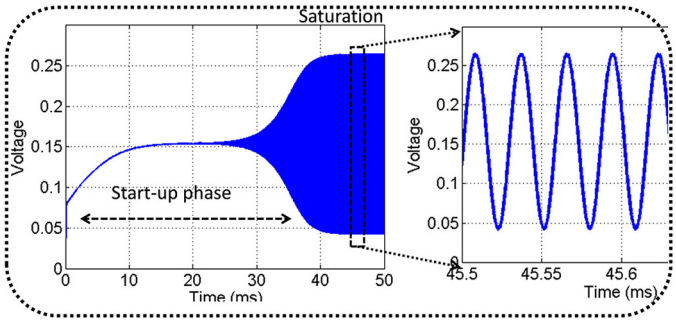
F4:1 Fig. 4. XTAL oscillator amplifier design and calibration control.



F5:1 Fig. 5. Performance of the amplifier characteristics showing $R_{\rm NEG}$ across 100 point Monte Carlo simulation and its bias current measured across 22 chips before
F5:2 and after calibration.

bias current. The longer length device also helps in reducing the variation of the device characteristics at lower voltages. Use of long $L_{\rm VT}$ transistors also helps in getting better gain and hence higher $R_{\rm NEG}$.

The amplifier was designed to operate in the subthreshold region with a V_{DD} of 0.3 V. Owing to the subthreshold region of operation, the amplifier bias current is sensitive to process variation. As a result, the negative resistance and power consumption of the amplifier can still show variation with process. At some process corners, the amplifier can consume higher power and give very high $R_{\rm NEG}$; and at other process corners, its $R_{\rm NEG}$ can be low, and it may fail to meet the oscillation criteria. We propose a calibration method to address this variation where we bias the amplifier with a fixed current. Equations (3) and (4) show that a fixed bias current will give a fixed $R_{\rm NEG}$ at a given temperature. Fig. 4(a) and (b) shows the calibration circuit. We set the drive strength of the amplifier transistors M_P and M_N using this circuit. The amplifier is enabled when ENP $= 0$ and ENN $= 1$. For calibration of M_N to a given drive strength, ENN and ENP are set to one. This enables the calibration circuit, where M_N gets connected to an external resistor through the switch M_{NC}. XI is connected to REF, which is selected to be at $V_{DD}/2$. The size of the transistor M_N is changed using successive approximation register (SAR) logic with the comparator in a feedback loop. This happens in the following way. XI and REF are set to $V_{DD}/2$ and the pull-down path is enabled, while the pull-up path is disabled. The external resistor R_C is connected to V_{DD}. If the drive strength of



F6:1 F6:2 Fig. 6. Simulation result of the XTAL oscillator circuit operating at 0.3 V V_{DD} with a reduced Q XTAL resonator.

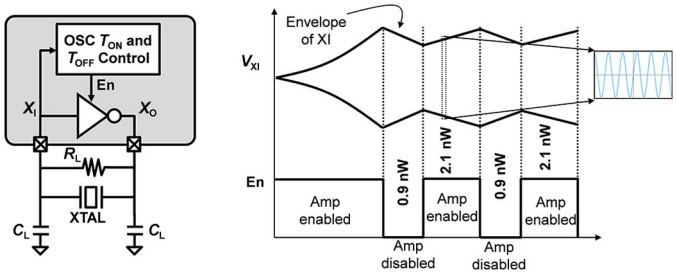
M_N is high, then it will pull down the XO node below REF, which will cause the comparator output to go low. This low signal sets the SAR logic to decrease the drive strength of the transistor M_N. The transistor M_N is realized using series connection of several 0.6 $\mu/10$ μ nMOS as shown in Fig. 4(a). The long transistors are connected in parallel with nMOS calibration switches connected to ground, where only one nMOS switch is on at a time to provide a given drive strength. The SAR logic reduces or increases the drive strength of MN by connecting more or fewer long transistors in series. The size of M_N is successively approximated, and it takes 5 clock cycles. This way M_N can be sized to the right drive strength. Similarly, M_P is sized by setting ENN and ENP to zero and connecting the external resistor to ground. We use an external resistance such that the amplifier can be sized to supply 5–20 nA of bias current, which provides enough drive strength to meet the criteria for oscillation. The calibration is performed at lower V_{DD} of 0.3 V. Fig. 5(a) shows the variation of $\mathrm{R_{NEG}}$ across a 100 point Monte Carlo simulation with and without calibration. The mean R_{NEG} of the amplifier without calibration is -70 kΩ with a 3σ variation of 36 kΩ, whereas the 3σ variation with calibration is 5.4 $k\Omega$. Fig. 5(b) shows the measurement of the amplifier bias current before and after calibration. It varies from 6 to 16 nA across several chips. After calibration, the 3σ variation of the amplifier current was brought down 0.9 nA with a mean of 10 nA. Fig. 6 shows the simulation result of the XTAL oscillator operating at 0.3 V V_{DD} with a power consumption of 2.2 nW. We achieve 2.2 nW power consumption for 30 kΩ XTAL. The power consumption of an XTAL with an ESR of 50 kΩ is going to be 5.6 nW at an R_{NEG} of -100 kΩ and 15 nW for a 90 kΩ XTAL. We use a reduced Q resonator for this simulation to reduce the start-up time and the simulation time. The Q is reduced by lowering the motional inductance and by increasing the motional capacitance of the resonator which has little impact on the required oscillation criteria.

IV. Amplifier Duty Cycling

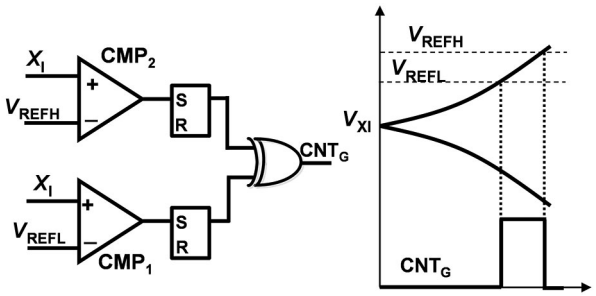
In order for the oscillator to start, $|R_{\mathrm{NEG}}| > \mathrm{ESR}$. The start-up time, the time the oscillator takes to reach the full amplitude, is also controlled by R_{NEG}. The higher the value of R_{NEG}, the faster will be the start-up [12]. However, a higher value of R_{NEG} means higher power consumption. The amplitude of oscillation saturates after start-up. After the oscillation saturates, the R_{NEG} of the amplifier decreases because of the nonlinearity in the circuit due to saturation, and effectively $|R_{\mathrm{NEG}}| = \mathrm{ESR}$ at saturation [11]. The saturation of oscillation creates higher harmonics, resulting in unnecessary power dissipation. While higher power is needed during start-up [12], it is not needed when the oscillation saturates. We propose further improvements in the design to save this power.

The energy of a XTAL oscillator is stored in its equivalent inductor and capacitors. After the saturation of oscillation, the stored energy in the XTAL's equivalent inductor and capacitor is saturated. After the saturation, if the amplifier is disabled, the oscillation will start decaying; and if we enable it again, it will start growing again. The power consumption becomes negligible when the oscillator is disabled. However, oscillation does not die right away and decays slowly, with the time constant given by R_{ESR} and L_m of the XTAL. The output of the XTAL oscillator is still useful and can be used to provide the clock when it is decaying. Therefore, the power consumption of a XTAL oscillator can be further reduced by switching the amplifier. In our design, we switch the amplifier periodically, while keeping the amplitude of oscillation high enough for the clock buffer circuit to detect the oscillation. The work in [15] also proposes a duty-cycling technique to reduce the power consumption of a 39 MHz XTAL oscillator. However, there are several differences between our implementation and the implementation of [15]. It implements a three stage amplifier to reduce the short-circuit current, which is a concern for high frequency oscillators. For low frequency oscillators such as a 32 kHz oscillator operating at 0.3 V V_{DD}, the short circuit current is small. Further, adding three stages of the amplifier in our oscillator will increase the power consumption without duty cycling as each stage will add power overheard. The second main difference between our implementation and [15] is that the control of switches to turn-off the oscillator is external while our implementation is built internally. The authors in [15] obtain the time of decay of oscillation using high-V_T inverters when they stop sensing the oscillations and use this information to turn the oscillator back on again. This implementation can bring the amplitude of oscillation low and cause higher jitter at the output. Also, it uses a fixed time to turn on the oscillator, and the oscillator remains in saturation for more than the required time. Our implementation proposes a method where both TG and TD are proportional to the growth and decay of the oscillation, which we will describe in the following sections. This information is obtained without significantly reducing the amplitude of oscillation. We obtain the correct duty-cycling ratio, and the jitter of our clock is not significantly higher as shown in Fig. 15.

Fig. 7 shows the concept of the control scheme. When the amplifier is disabled, the oscillation at XI will decay with a time constant (TD), which is determined by the R_{ESR} and L_m. When the amplifier is enabled, it grows with a time constant (TG), which is determined by $|R_{\mathrm{NEG}}| - R_{\mathrm{ESR}}$ and L_m [12]. For optimal power savings, the amplifier should be disabled for a time proportional to TD and enabled for a time proportional to TG, as shown in Fig. 7. A counter running on the oscillator output frequency is enabled when the amplitude crosses a



F7:1 Fig. 7. Circuit diagram and operation of oscillator duty cycling.



F8:1 Fig. 8. Circuit to obtain the time constant for the growth of oscillation TG.

set threshold. It counts until CNT_G and stops when the amplitude crosses a higher threshold. This gives us a digital output proportional to TG. Similarly, a CNT_D proportional to TD can be obtained. A clock with the period $(\mathrm{CNT}_G + \mathrm{CNT}_D)$ is obtained, with CNT_G as High and CNT_D as low, as shown in Fig. 7. The proposed technique enables a calibrated switching of the amplifier of the XTAL oscillator and helps in cutting down the power further down to a measured average power of 1.5 nW.

A. Obtaining Time of Growth of Oscillation

Fig. 8 shows the circuit to obtain the TG of the oscillation. It consists of comparators and SR flip-flop. Reference voltages V_{REFH} and V_{REFL} are used for one time calibration to obtain the TG of the oscillator. Threshold voltages $V_{\mathrm{REFH}} = 220$ mV and $V_{\mathrm{REFL}} = 200$ mV are applied at the negative terminal of the comparators, while XI is applied at the positive terminal. Once oscillation amplitude goes above V_{REFL}, the output of CMP_1 goes high, and corresponding SR flip-flop is set. This sets CNT_G to high. A counter is enabled using this signal to count. The amplitude of oscillation keeps on increasing. Once the oscillation crosses V_{REFH}, CMP_2 goes high and sets CNT_G to zero. This stops the counter and sets the value of the counter, which is proportional to the growth of oscillation. The value is digital and is stored, while the time constant circuit is disabled to save power.

B. Obtaining Time of Decay of Oscillation

Fig. 9 shows the circuit implementation for obtaining TD for the oscillator. The circuit is very similar to the circuit used for obtaining TG. It also enables a counter, which counts when XI

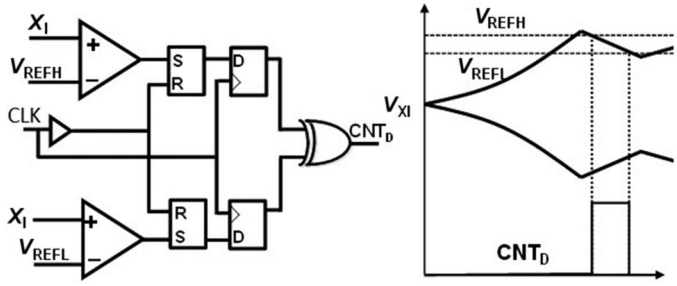


Fig. 9. Circuit to obtain the time constant for the decay of oscillation T_D. F9:1

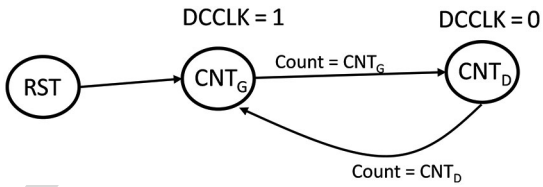


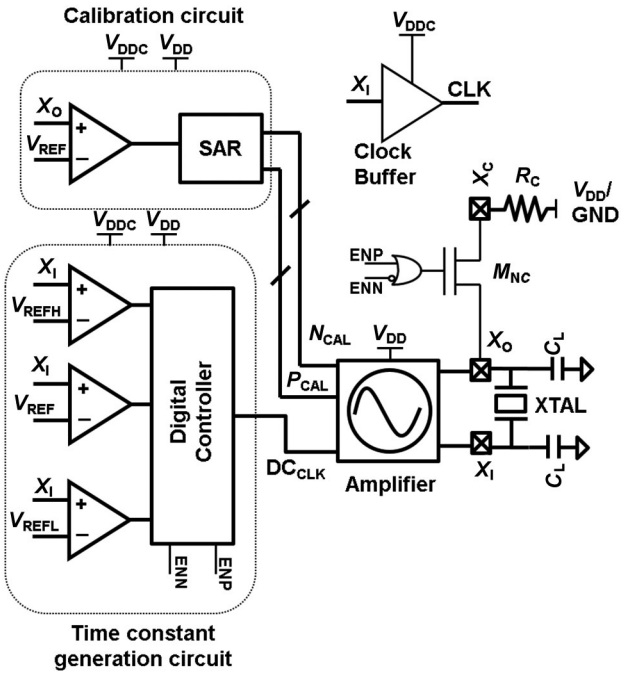
Fig. 10. Digital state machine for generating duty-cycling clock $\mathrm{DC}_{\mathrm{CLK}}$. F10:1

is between V_{REFH} and V_{REFL}. While TG is obtained when the amplifier is enabled, TD is obtained when it is disabled. Both TG and TD are stored digitally, and their corresponding circuits are disabled to save power. After obtaining TG and TD, the oscillator control turns on the amplifier for time = TD and turns it off for time = TG.

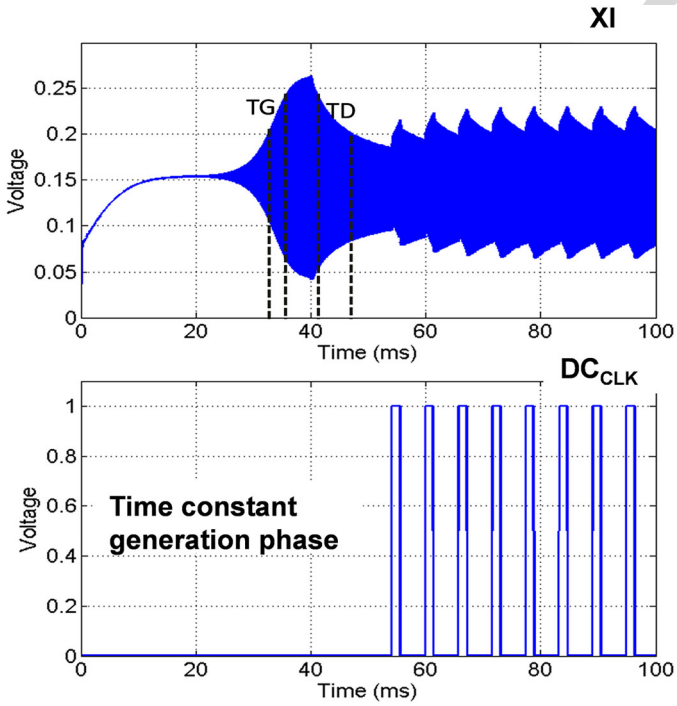
Fig. 10 shows the digital controller for generating the duty-cycling clock $\mathrm{DC}_{\mathrm{CLK}}$ for the oscillator. A counter running on oscillator output frequency is enabled for the duty-cycling mode. It counts for CNT_G and sets $\mathrm{DC}_{\mathrm{CLK}}$ high in that state. It then goes to second state and counts for CNT_D and sets $\mathrm{DC}_{\mathrm{CLK}}$ low for that state. It sets both TG and TD, and a running $\mathrm{DC}_{\mathrm{CLK}}$ is realized.

C. Complete Circuit Architecture

Fig. 11 shows the complete circuit diagram of the proposed XTAL oscillator circuit. First, the calibration of the amplifier is performed, which can be done once after manufacturing. The calibration circuit sets the drive strength of the amplifier and compensates for the process variation. After the calibration, the time constant generation circuit obtains the time of growth (TG) and time of decay (TD) of the oscillator. These time constants are used to configure the clock ($\mathrm{DC}_{\mathrm{CLK}}$) to switch the amplifier on and off. The duty cycle of $\mathrm{DC}_{\mathrm{CLK}}$ is determined by TG and TD with high time = TG and low time = TD. Both the calibration circuit and the time constant generation circuit are operated at higher power supply, V_{DDC} at 0.9 V. The power consumption of the time constant generation and calibration circuit is 4 μW. We perform calibration and time constant generation only once at 0.3 V V_{DD} and at room temperature. Once the $\mathrm{DC}_{\mathrm{CLK}}$ is configured, the time constant generation circuit is powered down. Similarly, the calibration circuit is powered down after calibration and all the digital bits are stored. This eliminates the power overhead of the calibration circuit or time constant generation circuit. The power consumption



F11:1 Fig. 11. Complete circuit architecture of the ULP XTAL oscillator.



F12:1 Fig. 12. Simulation of the duty-cycle XTAL oscillator at 0.3 V V_{DD}.

is given by the amplifier with duty cycling. A clock buffer is used along with a level converter to up-convert the clock to higher voltage if needed. The level converter implements an ULP converter [13] and consumes less than 1 nW for level converting the XTAL output from 300 mV to 0.9 V. Fig. 12 shows the simulation result of the duty-cycling XTAL oscillator. After time constant generation phase, the XTAL operates in the duty-cycling mode, providing a stable clock with a power consumption of 1.5 nW.

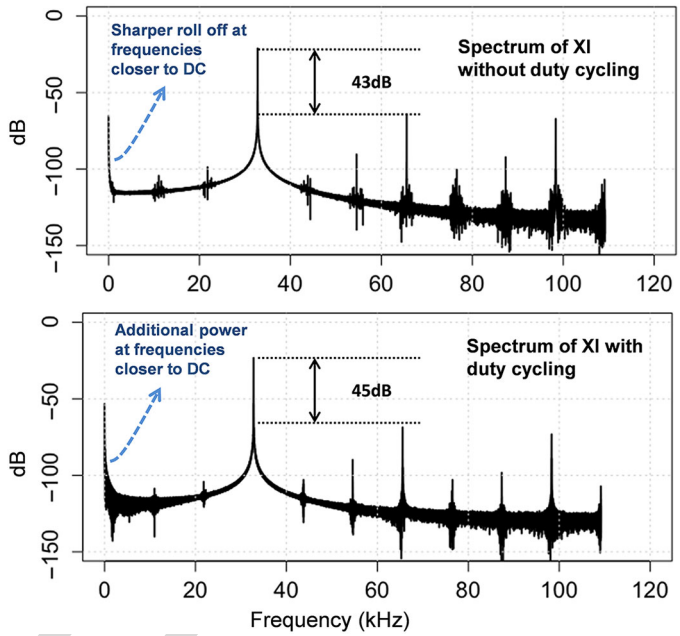
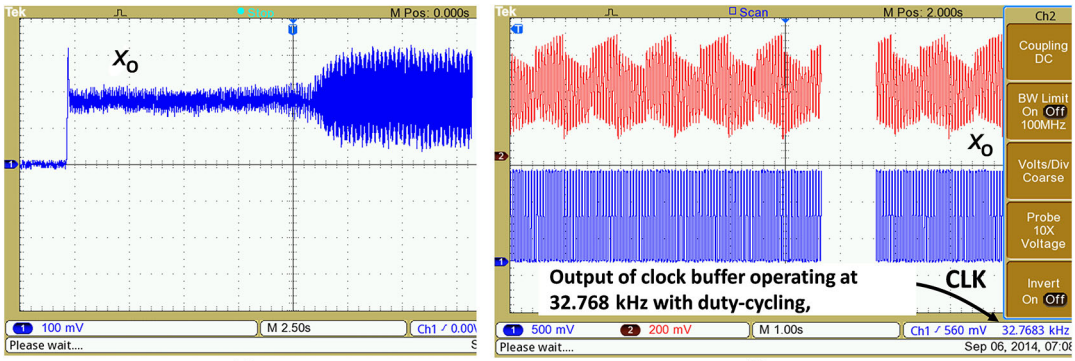


Fig. 13. Spectrum of XI with and without duty cycling. F13:1

The time constants TG and TD are both multiples of the clock period. In our design, the 32.768 kHz clock will be an exact multiple of DC_{CLK}, which is derived from the XTAL output. Further, the high Q of the XTAL makes TG and TD really large, and the frequency of DC_{CLK} is between 2 and 50 Hz. Fig. 13 shows the spectrum of XI with and without duty cycling. The duty-cycling spectrum shows slightly higher power in frequencies closer to DC. This will result in increase in jitter, which is shown in Fig. 15.

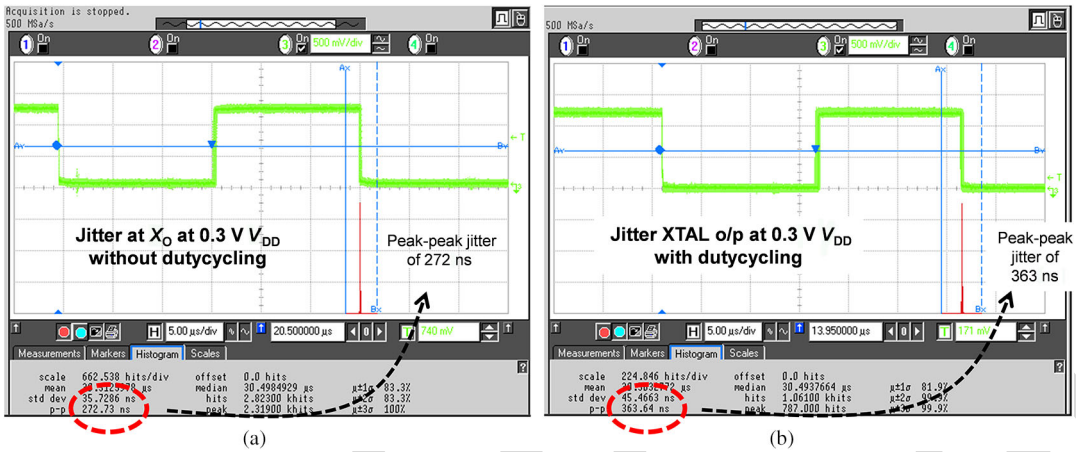
D. Nonlinear Effects

We use small signal analysis to realize the oscillation criteria, where the negative resistance of the amplifier is calculated at the bias condition of the amplifier. The small signal analysis gives the accurate behavior of the oscillator when the amplitude of oscillation is small. However, nonlinearity in the circuit manifests when the amplitude of oscillation starts becoming large. As the amplitude of oscillation increases, the gain of the amplifier decreases as transistors inside the amplifier can no longer stay in saturation. The decrease in the gain will start reducing the effective negative resistance of the amplifier. The higher value of negative resistance over XTAL oscillator's ESR during start-up causes an exponential growth of amplitude. However, as the amplitude increases, the gain of the amplifier drops, causing a decrease in the negative resistance. At saturation, the effective negative resistance (large signal value) of the amplifier becomes equal to the ESR of the XTAL and the circuit reaches steady state condition. Two main concerns are highlighted with respect to using an inverter-based XTAL oscillator in [8]. The first concern is the finite capacitance looking at the output of the power supply used for the inverter-based amplifier. The finite capacitance on the power supply results in the distortion leading to poor frequency stability. Since we use the XTAL oscillator in an energy harvesting application, the power



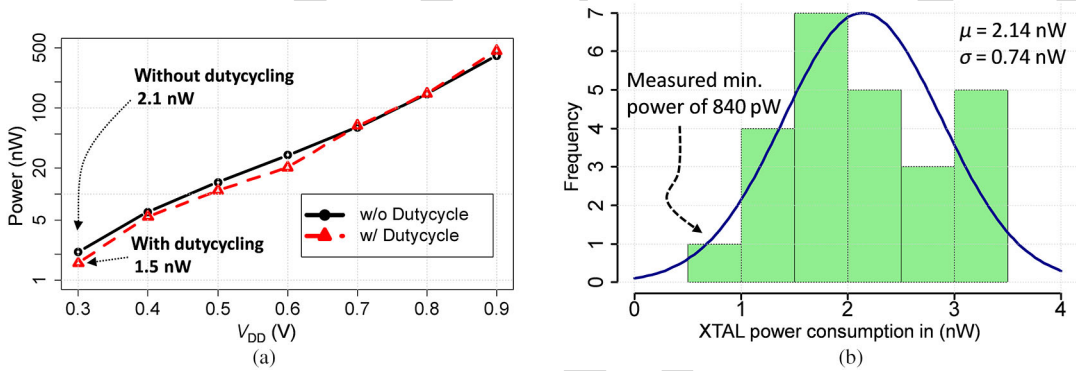
(a) (b)

F14:1 Fig. 14. Measured output waveform of the XTAL oscillator circuit. (a) Start-up of the XTAL oscillator at 0.4 V V_{DD}. (b) Measurement of the waveform at XO
F14:2 with duty-cycling and producing the output clock at 32.768 kHz.



(a) (b)

F15:1 Fig. 15. Measurement of jitter at clock buffer out CLK without duty-cycling and with duty-cycling techniques.



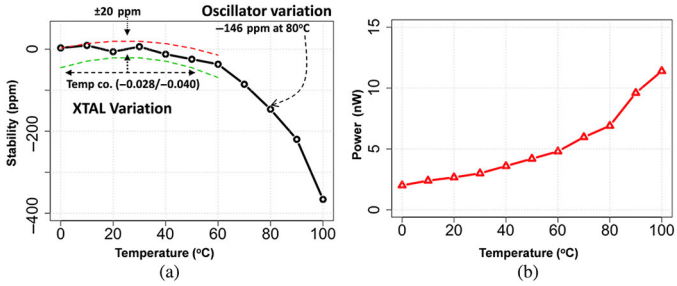
(a) (b)

F16:1 Fig. 16. Measured power consumption of XTAL.

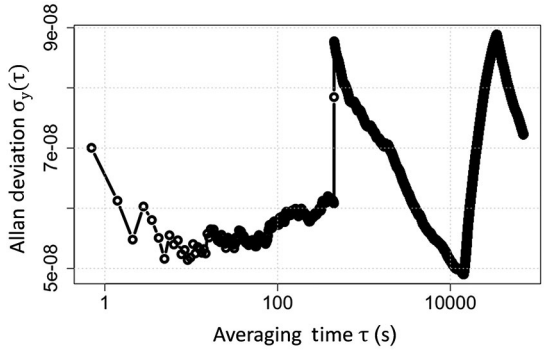
supply will see 100's of µF to few mF of cap at the output. With lower power consumption and large output capacitance on the power supply, we did not see increased instability in the output frequency of the oscillator. The second concern is with respect to power. Authors in [8] point out that higher power in the oscillator results in distortion due large value of gm of the amplifier. This is a concern even with current source-based amplifier. Fig. 13 shows that the power in the second harmonic is roughly 43 dB below the fundamental at 0.3 V V_{DD}. At higher voltage of 0.9 V V_{DD}, we see that second harmonic is roughly 34 dB below the fundamental, resulting in an increase in relative power in harmonics due to higher power. The main advantage of inverter-based oscillator is that the trans-conductance of both nMOS and pMOS are added, which results in overall lower power consumption for the same negative resistance.

V. Measurement Results

The proposed XTAL circuit was implemented in a 130 nm CMOS process. It uses a 3 GΩ external biasing resistor. The XTAL resonator used for this circuit has a Q of 90,000, an ESR of 30 kΩ, and a C_L of 6 pF. The XTAL's performance was

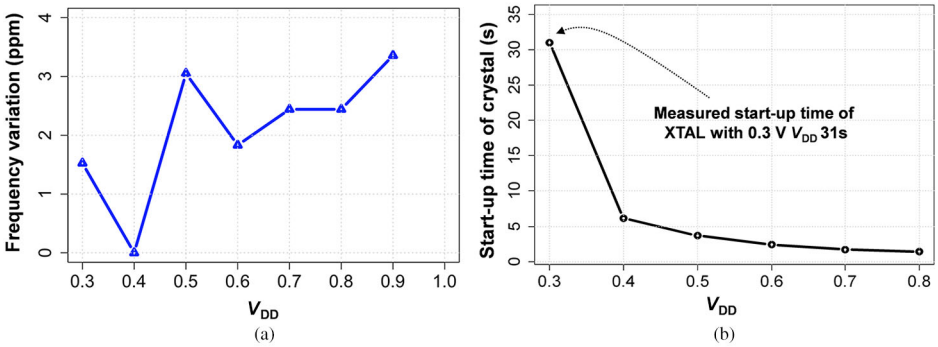


F17:1 Fig. 17. Measured stability and power of the XTAL with temperature, w/o duty
F17:2 cycling, 0.3 V V_{DD} shows stability of 1.87 ppm/°C for a temperature variation
F17:3 of 0 °C–80 °C.

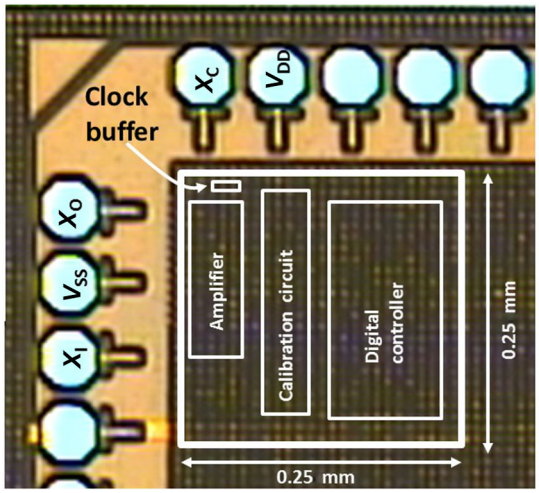


F18:1 Fig. 18. Allan deviation measurement of the XTAL output with duty cycling at
F18:2 0.3 V V_{DD} for approximately 20 h.

measured from V_{DD} of 0.3–0.9 V with a temperature variation from 0 °C to 100 °C. Our measurements were performed with a Keithly power supply with a 2.2 mF capacitance on the supply. Fig. 14(a) shows the measured start-up waveform at XO of the XTAL at 0.4 V V_{DD}. The operation of the XTAL at 0.3 V V_{DD} was measured indirectly by monitoring the clock-buffer output but the waveform at XO cannot be produced at this voltage because of the loading effects from the measurement instruments. Fig. 14(b) shows the measured waveform at XO with duty-cycling technique. The output waveform shows that oscillation is sustained with duty cycling and that the output clock provides a clock with a period of 32.768 kHz. Fig. 15 also shows the measurement of jitter at the output of the clock buffer. The RMS jitter without duty cycling is 272 ns and with duty cycling is 363 ns. Fig. 16(a) shows the power consumption measurement of the XTAL by varying V_{DD}. The measured average power consumption of the XTAL across 25 chips is 2.1 nW without duty cycling and 1.5 nW with duty cycling at room temperature and 0.3 V V_{DD}. The proposed technique does not show significant power improvement at higher V_{DD}. This is because the bias current at higher V_{DD} is much higher than required for oscillation. The output of the oscillator stays well below the full-rail with the duty cycling technique which increases the power consumption because of the short-circuit current in the amplifier as well as in the clock buffer. The overhead of the short-circuit current reduces the benefit of duty cycling at higher V_{DD}. We can save more power, if we configure the oscillator for lower power at higher V_{DD} where duty-cycling technique will show improvement as the short circuit current in the amplifier will decrease. We also configured the XTAL for minimum power consumption required for a sustained oscillation. Fig. 16(b) shows the measured minimum mean power consumption for a sustained oscillation without duty cycling across 25 chips is 2.1 nW with a sigma of 0.71 nW. Measurement for one chip showed a minimum power consumption of 840 pW, where it is approaching the theoretical power consumption limit set by (3) and (4). Fig. 17(a) shows the stability of the oscillator over 0 °C–100 °C at 0.3 V V_{DD}. The chip was calibrated at 0.3 V V_{DD} and room temperature. We maintained this configuration for varying temperature and power supply measurements. Our frequency stability is -146 ppm at 80°C. Fig. 17(a) also shows the variation of the XTAL. Our frequency stability is within the bounds of XTAL variation. The measured frequency stability from 0 °C to 80 °C is 1.85 ppm/°C. The output frequency with duty-cycling technique is 2.5 ppm below the frequency of oscillation without duty cycling at 20 °C. The stability of the overall system is -150 ppm between 0 °C and 80 °C. Fig. 18 shows the measurement of Allan deviation of the XTAL with duty cycling operating at 0.3 V V_{DD}. The measurements were taken with a τ of 0.7 s for approximately 20 h in lab environment. The measurement shows Allan deviation of less than 10^{-7}. Fig. 19(a) shows the variation of the oscillator's frequency with V_{DD}. The power supply variation of our oscillator is less than 7 ppm/V. Fig. 19(b) shows the measured start-up time of the XTAL. The measurement for the start-up time were taken with the oscillator configured for minimum power consumption at 0.3 V V_{DD}. The worst case start-up time is 31 s for 0.3 V V_{DD}. The lower margin on ESR gives higher start-up time. However, our circuit can also start-up in a higher current configuration with all the calibration bits programmed high, which can reduce the start-up time. The circuit can then make use of the lower power configuration. Fig. 20 shows the die photo and the implementation of the XTAL oscillator. The area of XTAL oscillator is $0.0625\ \mathrm{mm}^2$. The Q of the XTAL resonator used for the XTAL oscillator is 90,000, and its ESR is 30 kΩ. We used an external 2 pF load capacitor, which combines with parasitic load capacitance to result in an oscillation frequency of 32.7683 kHz at room temperature. Table I shows the comparison summary of the proposed XTAL circuit with previous work. Our XTAL oscillator circuit consumes 1.5 nW of power and has an area of $0.0625\ \mathrm{mm}^2$. It has over 26% lower power compared to [7] and over 3.7× lower power and 8× lower area compared to [10]. We operated the XTAL circuit at 0.3 V V_{DD}, with a duty-cycling technique. The circuit in [7] uses a self-charging technique to operate the XTAL at 0.15 V V_{DD} to achieve a power consumption of 1.89 nW. The circuit in [10] uses a DLL-based technique and employs two power supplies and two grounds for the amplifier stage. Our circuit uses a single power supply for the amplifier. Previously reported work achieves a power consumption of 22 nW [9] by reducing the amplitude of oscillation. We reduce the amplitude of oscillation by operating the circuit at 0.3 V V_{DD}. The proposed circuit provides a low power, lower area XTAL oscillator circuit. It applies lower voltage design in conjunction with a duty-cycling technique to achieve lower power suitable for ULP devices in IoT networks.



F19:1 Fig. 19. (a) Measured frequency variation with V_{DD}. (b) Measured start-up time of XTAL with V_{DD}.



Parameter	Value
Technology	130 nm bulk CMOS
Total area	250 µm × 250 µm
XTAL's ESR	30 kΩ
XTAL's *Q*-factor	90 000
XTAL's C_m	3.5 fF
XTAL's shunt cap	1.5 pF
C_L	6 pF*
Feedback res. (R_L)	3 GΩ
Calibration res. (R_C)	15 MΩ
XTAL freq. tolerance	± 20 ppm

**The load capacitor includes the parasitic capacitance as well as external capacitance*

F20:1 Fig. 20. Die photo of the XTAL circuit and parameters for the configuration in Fig. 1.

T1:1 TABLE I

T1:2 COMPARISON SUMMARY OF THE DUTY-CYCLED OSCILLATOR WITH PREVIOUS LOW-POWER XTAL

	[7]	[10]	[9]	[14]	This work
Operating frequency	32 kHz	32 kHz	32 kHz	32kHz	32kHz
Area (mm^2)	0.03	0.3	N/A	25	0.0625
Power consumption (nW)	1.89 @0.15V V_{DD} 10 @0.3V V_{DD}	5.58	22	220	1.5 @ 0.3V V_{DD}
Operating V_{DD}(V)	0.15–0.5	0.92–1.8	0.71	3	0.3–0.9
Number of power/Gnd	1/1	2/2	1/1	1/1	1/1
Amplitude of oscillation	N/A	100 mV	65 mV	N/A	230 mV
Temperature stability	–48.8 ppm –20–80°C	–133 ppm –20–80°C	N/A	N/A	–146 ppm (w/o dutycycling) –150 ppm (w dutycycling) 0–80°C
Power supply variation	85 ppm/V	N/A	N/A	2 ppm/V	7 ppm/V
Technology	28 nm	0.18 µm	2 µm	2 µm	0.13 µm

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QUERIES

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Q3: Please provide year of publication for Ref. [12].

A 1.5 nW, 32.768 kHz XTAL Oscillator Operational From a 0.3 V Supply

Aatmesh Shrivastava, Divya A. Kamakshi, and Benton H. Calhoun

***Abstract*—This paper presents an ultra-low power crystal (XTAL) oscillator circuit for generating a 32.768 kHz clock source for real-time clock generation. An inverting amplifier operational from 0.3 V V_{DD} oscillates the XTAL resonator and achieves a power consumption of 2.1 nW. A duty-cycling technique powers down the XTAL amplifier without losing the oscillation and reduces the power consumption to 1.5 nW. The proposed circuit is implemented in 130 nm CMOS with an area of 0.0625 mm^2 and achieves a temperature stability of 1.85 ppm/°C.**

***Index Terms*—32 kHz XO, clock source, crystal (XTAL) oscillator, Internet of Things (IoT), real-time clock (RTC), subthreshold, ultra-low power (ULP).**

I. Introduction

ULTRA-LOW power (ULP) systems such as wireless sensor nodes (WSNs) for emerging Internet of Things (IoT) applications spend a large portion of their time in inactive or idle mode to save power. A typical operation of a ULP system constitutes a short burst of activity followed by a long idle time. The short burst of activity consumes higher power, whereas the power consumption in idle mode is relatively small. Spending a large time in the idle mode saves energy and can help with recharging the storage capacitor of energy harvesting ULP systems [1] from low energy ambient harvesting sources. To maximize idle time while remaining functional in a larger interconnected IoT network, these systems require precise clock to synchronize and wake-up the system at regular intervals. A real-time clock (RTC) utilizing an ULP oscillator is often used for this purpose. The total power consumption of such a system may be determined by the power consumption of the RTC. To reduce the power consumption and to increase the life-time of the system, the power consumption of the RTC needs to be reduced. In this paper, we present a 32.768 kHz crystal (XTAL) oscillator for RTC applications with a power consumption of 1.5 nW.

Widely varied circuit architectures ranging from on-chip oscillators to off-chip XTAL oscillators exist for the implementation of the RTC in an ULP system. A precision CMOS relaxation oscillator is presented in [2]. It achieves a temperature stability of 60 ppm/°C, but its power consumption is 45 μW for a 14 MHz clock. Further, the oscillator shows a power supply variation of 16 ppm/mV. A 150 nW, 100 kHz on-chip oscillator achieves a temperature stability of 5 ppm/°C for a temperature range of 20 °C–40 °C and 14 ppm/°C for a temperature range of 20 °C–70 °C [3]. The power supply variation of this oscillator is 0.1%/mV. The temperature stability and the power consumption of the oscillator make it suitable for ULP applications, but it requires a very controlled power supply. On-chip oscillators, using the gate leakage current, have been proposed in [4]–[6]. These designs employ calibration for temperature compensation and achieve a best temperature stability of 32 ppm/°C. The power supply variation of this oscillator is 0.42%/mV. Further, these oscillators can operate only at very low frequency (0.1–10 Hz) due to the low magnitude of gate-leakage current. The lower output frequency and higher power supply variation limits their usage for precise RTC applications.

A XTAL oscillator provides a very precise output frequency ($\sim 5-20$ ppm/°C) that is not affected by process or power supply variation by using an off-chip electro-mechanical XTAL resonator. Although off-chip components can increase the cost and volume of the system, XTALs are now being explored for ULP systems that require precise timing for wake-up or synchronization of a WSN in an IoT network. The power consumption of the XTAL used in ULP systems must be very small. Recent work on the design of 32 kHz XTAL oscillators show power consumption in the single digit nW range [7], [10], making it possible to use them for ULP applications. Power consumption of XTAL oscillators can be reduced by lowering the amplitude of oscillation by operating at lower voltages. Low power electronic watches use this technique to operate XTAL oscillator circuits in the subthreshold or weak inversion region of operation of the transistors [8]. The XTAL oscillator circuit proposed in [9] achieves a power consumption of 22 nW operating with a power supply (V_{DD}) around 600 mV. A delay locked loop (DLL)-based XTAL [10] achieves a power consumption of 5.58 nW. It also achieves lower swing to reduce the power consumption in the XTAL's effective series resistance (ESR). However, to reduce the power consumption and to maintain low swing for oscillation, it needs two power supplies and two grounds. It also requires a large area for its implementation. A self-charging XTAL design reduces the power consumption to 1.89 nW [7]. In this circuit, XI and XO are operated in a self-charging loop, where both XI and XO are charged based on the operating phase of the oscillator using only the parasitic load capacitors. In conventional designs, the input of the oscillator XI is obtained from XO as a filtered output through

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the high quality XTAL. The spectrum of XI will contain only the resonance frequency of the oscillator. However, the self-charging scheme [7] charges XI too to maintain the oscillation. The circuit used for charging XI can introduce additional frequency components in XI, which may degrade the spectrum of the oscillator.

In this work, we present a 1.5 nW, 32 kHz XTAL oscillator, which operates the XTAL with a feedback amplifier operating at 300 mV. We propose a technique of duty cycling the XTAL oscillator in conjunction with operating them in a subthreshold region. We achieve a measured average power consumption of 1.5 nW across 25 chips. In Section II, we present the operation of the XTAL. Section III presents the low power amplifier design and Section IV presents the duty-cycling technique. Section V presents measurement results.

II. XTAL Operation

An XTAL is an electromechanical resonator that resonates at its natural frequency when excited with electrical energy. Fig. 1(a) shows a conventional XTAL oscillator circuit. The equivalent circuit of an XTAL consists of a series RLC circuit with a parasitic parallel capacitor C_p. The frequency of oscillation is mainly determined by the motional inductor L_m and capacitor C_m. The ESR is the energy dissipating component of the XTAL. The inverting amplifier provides the negative resistance that overcomes the loss from ESR and pumps energy into the XTAL, making it oscillate at its natural frequency. The output frequency of the XTAL oscillator is very precise, and its stability is usually specified at parts per million or per billion (ppm/ppb). The extremely precise output frequency of XTAL oscillators makes them a natural choice for implementing clocks. Further, the frequency of oscillation is largely independent of voltage and process variation.

A. Theoretical Analysis for Low-Power XTAL Oscillation

The XTAL circuit can be made to oscillate in series or parallel mode. Parallel mode is the commonly employed mode of oscillation. In parallel mode, the XTAL is connected with an inverting amplifier with two load capacitors connected in parallel (C_L), as shown in Fig. 1(a). In parallel mode, the XTAL appears as an inductor and oscillates with the load capacitors (C_L). In order to oscillate, the circuit needs to meet the Barkhausen or the negative resistance criteria of oscillation. For negative resistance oscillation criteria, the amplifier needs to present a negative resistance ($R_{\rm NEG}$) at resonant frequency, whose absolute value should be greater than the XTAL's ESR ($R_{\rm ESR}$) [11] ($|R_{\rm NEG}| > R_{\rm ESR}$). We derive a theoretical analysis for a low power XTAL oscillator from the work presented in [8]. Fig. 1(b) shows a hypothetical three point oscillator. The negative resistance of the oscillator can be derived from [8, eq. (16)] as follows:

$$R_{\rm NEG} = \frac{-g_m C_L^2}{(g_m C_P)^2 + \omega^2 (C_L^2 + 2C_P C_L)^2}$$
$$R_{\rm NEG} = \frac{-g_m}{(g_m C_P / C_L)^2 + \omega^2 (C_L + 2C_P)^2}. \quad (1)$$

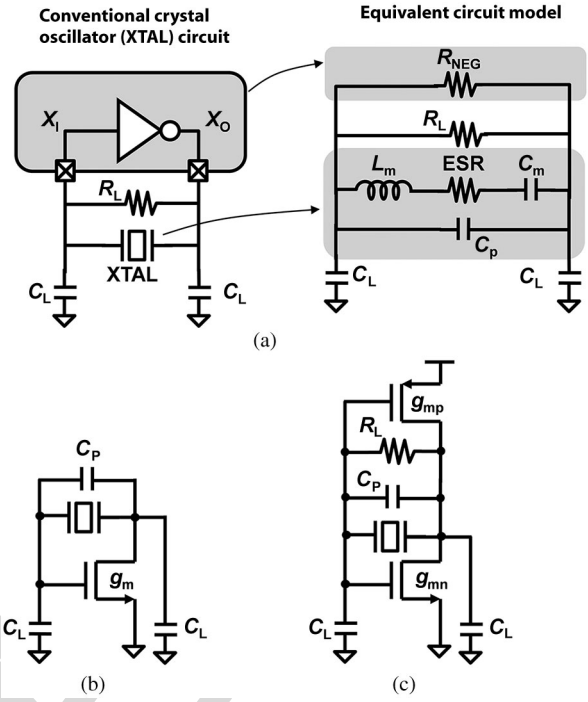


Fig. 1. (a) Conventional XTAL oscillator circuit and its equivalent representation. (b) Analysis of a three-point oscillator. (c) Practical implementation of XTAL oscillator with an inverter (push–pull oscillator). F1:1 F1:2 F1:3

Since $(g_m C_P / C_L)^2 \ll \omega^2 (C_L + 2C_P)^2$

$$R_{\rm NEG} = \frac{-g_m}{\omega^2 (C_L + 2C_P)^2}. \quad (2)$$

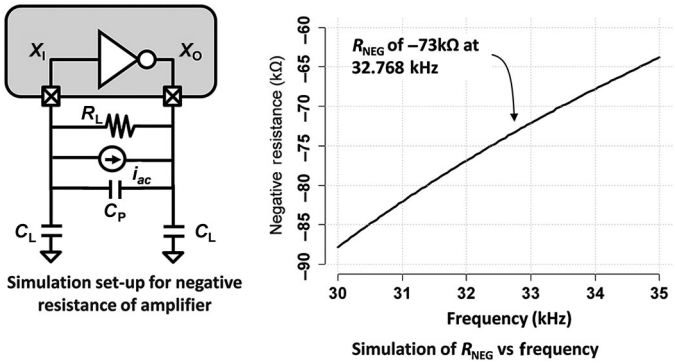
For an inverter-based oscillator, as shown in Fig. 1(c), the transconductance of both n*MOS* and p*MOS* devices will add, and the $R_{\rm NEG}$ can be approximately written as

$$R_{\rm NEG} = \frac{(-g_{mn} - g_{mp})}{\omega^2 (C_L + 2C_P)^2}. \quad (3)$$

For a device operating in subthreshold, the transconductance is given by

$$g_m = \frac{I_D}{n V_t} \quad (4)$$

where I_D is the drain source saturation current, n is the subthreshold slope approximately equal to 1.2, and V_t is the thermal voltage, which is 26 mV at room temperature. An n*MOS* biased at 7 nA of $\rm I_D$ gives a g_m of $2.24 \times 10^{-7} \Omega^{-1}$. Using the same value for g_{mn} and g_{mp}, (3) gives an $R_{\rm NEG}$ of -180 kΩ for a C_L of 6 pF and C_P of 1 pF. A power limit can be derived from (3) and (4) for various conditions. Assuming that a -60 kΩ $R_{\rm NEG}$ is sufficient for oscillation for a 30 kΩ ESR XTAL, an inverter running at 0.3 V can realize oscillation at 0.7 nW for a C_L of 6 pF. If a lower C_L value of 3 pF is used, then it is possible to achieve oscillation at 0.28 nW. Further, if one can realize an oscillator circuit at 150 mV V_{DD} as used in [7], then the power required to achieve oscillation is 140 pW with



F2:1 Fig. 2. Design method for the XTAL oscillator circuit.

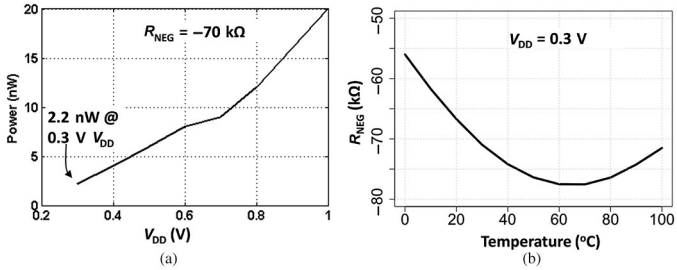


Fig. 3. (a) Simulation of XTAL oscillator power consumption across V_{DD} F3:1
with a fixed negative resistance of amplifier at -70 kΩ. (b) Simulation of F3:2
negative resistance of the amplifier with temperature at 0.3 V V_{DD}. F3:3

margin. In order to just barely meet the oscillation criteria, the power required sits at 70 pW.

B. Practical Design of a Low-Power XTAL Oscillator

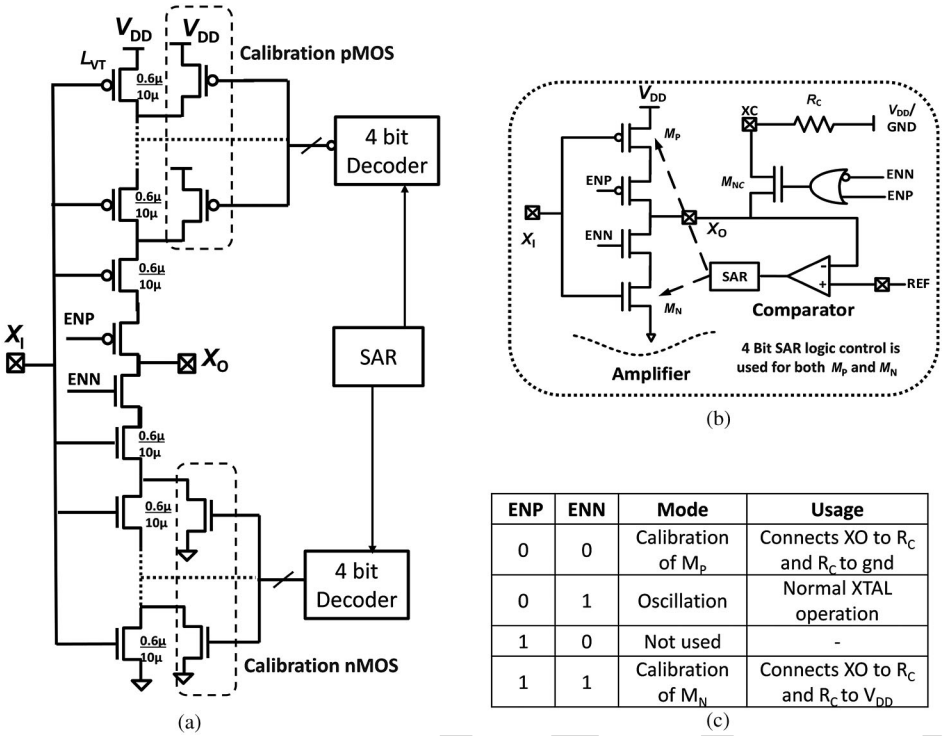
The preceding section showed the theoretical power required to achieve oscillation. However, several practical issues can reduce the $R_{\rm NEG}$ at subthreshold current levels. In this section, we present the practical design method for realizing the required $R_{\rm NEG}$ for oscillation, and Fig. 2 shows the design method. In this circuit, XTAL is removed from the oscillator, and an *ac* current source is connected across the amplifier terminal. The inverting amplifier presents an impedance to the applied ac current, which will have a real component at the oscillation frequency. The real component is the negative resistance ($R_{\rm NEG}$) of the amplifier at resonance. The value of $R_{\rm NEG}$ is a function of frequency. Fig. 2 shows the simulation of the $R_{\rm NEG}$ of the amplifier across frequency for a C_L of 6 pF and a C_P of 1 pF. The ESR of the XTAL oscillator at 32.768 kHz is typically in the range of 30 kΩ. The g_{mn} and g_{mp} of our oscillator is $1.12 \times 10^{-7}\Omega^{-1}$ and $1.16 \times 10^{-7}\Omega^{-1}$, respectively, at a bias current of 7 nA and V_{DD} of 0.3 V. Plugging these values in (3) yields a $R_{\rm NEG}$ of -90 kΩ. However, Fig. 2 shows that we can achieve a $R_{\rm NEG}$ of -73 kΩ. Further, the start-up time of the XTAL oscillator is in the range of $\sim$1 s because of the high quality factor (Q) of the XTAL resonator. The $R_{\rm NEG}$ of the amplifier also controls the start-up time, and a negative resistance with higher magnitude will reduce the start-up time of the XTAL [12].

The power consumption of the XTAL oscillator is determined by the XTAL and the amplifier. XTAL's ESR dissipates energy in the form of heat loss, as Joule's heating, which depends on the amplitude of oscillation. To reduce the power consumption of the XTAL oscillator, the amplitude of oscillation is often reduced. This can be done by operating the amplifier in the subthreshold region [8], [9]. In this paper, we propose a 32 kHz XTAL oscillator circuit that consumes 1.5 nW of power. We first operate the XTAL oscillator in subthreshold at 0.3 V V_{DD} to reduce the power consumption to 2.2 nW. We further reduce the power by applying a duty-cycling technique to turn-off the amplifier often. This technique brings down the over-all power consumption of the XTAL oscillator to 1.5 nW, improving the state-of-the-art by over 26%.

III. Low Power Amplifier Design

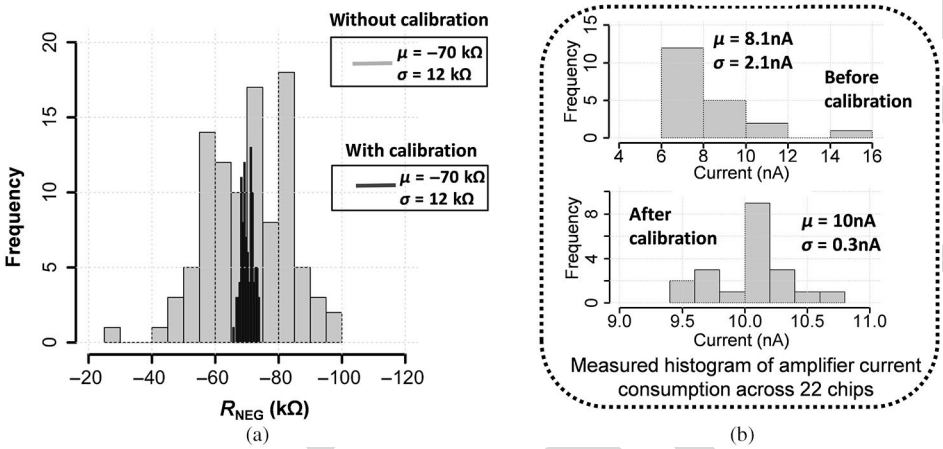
In this section, we present the design of the low power amplifier circuit. Various inverting amplifier architectures can be used to implement the amplifier. A simple push-pull inverter with a large bias resistor, as shown in Fig. 1, is one of the design options and is commonly used because it is single stage and hence consumes least amount of power [9]. However, the inverter circuit needs to be designed properly to meet the oscillation criterion. At lower drive strength (smaller sizes for *n*MOS and *p*MOS), the $R_{\rm NEG}$ of the amplifier is low and cannot meet the oscillation criterion. Increasing the size increases the $R_{\rm NEG}$. After a certain size, the $R_{\rm NEG}$ starts decreasing again because of the self-loading in the inverter through the gate-drain capacitance, C_{GD} (Miller-effect). Also, increasing the size of the inverter increases the power consumption. Therefore, the inverter needs to be sized properly for the power consumption, as well as for $R_{\rm NEG}$. Further, the power consumption can also be reduced by operating the amplifier circuit at a lower V_{DD}. At lower V_{DD}, the amplifier device sizes are typically bigger than the sizes for higher V_{DD}. However, the overall power consumption decreases. Fig. 3(a) shows the power consumption of the amplifier circuit designed to provide a fixed negative resistance of -70 kΩ at 32 kHz for different $V_{DD}s$ with a C_L of 6 pF and C_P of 1 pF. The power consumption increases with the voltage almost linearly. This is largely because the bias current of the amplifier almost remains the same for a given $R_{\rm NEG}$, which can be confirmed by inspecting equations (3) and (4). As a result, power increases because of the increase in the V_{DD}. Therefore, the oscillator needs to be operated at a lower V_{DD} to reduce the power. Further, the g_m of the amplifier is a weak function of temperature, so the $R_{\rm NEG}$ does not vary a lot with temperature as shown in Fig. 3(b). Our amplifier consumes 5–10 nA of quiescent current during start-up, which decreases after the saturation of oscillation. The power consumption of the XTAL oscillator is 2–10 nW at 0.3 V V_{DD}.

Fig. 4(a) shows the circuit diagram of the proposed amplifier. We use low threshold ($L_{\rm VT}$) transistors with longer length to implement the amplifier. $L_{\rm VT}$ transistors give better performance at 0.3 V V_{DD}, owing to the lower threshold voltage, while a longer length of the transistor helps in reducing the



ENP	ENN	Mode	Usage
0	0	Calibration of M_P	Connects XO to R_C and R_C to gnd
0	1	Oscillation	Normal XTAL operation
1	0	Not used	-
1	1	Calibration of M_N	Connects XO to R_C and R_C to V_{DD}

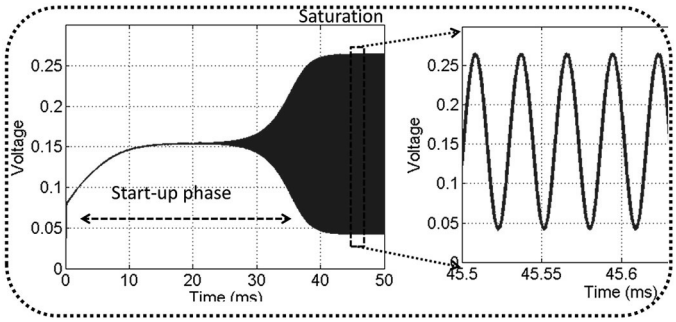
F4:1 Fig. 4. XTAL oscillator amplifier design and calibration control.



F5:1 Fig. 5. Performance of the amplifier characteristics showing $R_{\rm NEG}$ across 100 point Monte Carlo simulation and its bias current measured across 22 chips before
F5:2 and after calibration.

bias current. The longer length device also helps in reducing the variation of the device characteristics at lower voltages. Use of long $L_{\rm VT}$ transistors also helps in getting better gain and hence higher $R_{\rm NEG}$.

The amplifier was designed to operate in the subthreshold region with a V_{DD} of 0.3 V. Owing to the subthreshold region of operation, the amplifier bias current is sensitive to process variation. As a result, the negative resistance and power consumption of the amplifier can still show variation with process. At some process corners, the amplifier can consume higher power and give very high $R_{\rm NEG}$; and at other process corners, its $R_{\rm NEG}$ can be low, and it may fail to meet the oscillation criteria. We propose a calibration method to address this variation where we bias the amplifier with a fixed current. Equations (3) and (4) show that a fixed bias current will give a fixed $R_{\rm NEG}$ at a given temperature. Fig. 4(a) and (b) shows the calibration circuit. We set the drive strength of the amplifier transistors M_P and M_N using this circuit. The amplifier is enabled when $\rm ENP = 0$ and $\rm ENN = 1$. For calibration of M_N to a given drive strength, ENN and ENP are set to one. This enables the calibration circuit, where M_N gets connected to an external resistor through the switch M_{NC}. XI is connected to REF, which is selected to be at $V_{DD}/2$. The size of the transistor M_N is changed using successive approximation register (SAR) logic with the comparator in a feedback loop. This happens in the following way. XI and REF are set to $V_{DD}/2$ and the pull-down path is enabled, while the pull-up path is disabled. The external resistor R_C is connected to V_{DD}. If the drive strength of



F6:1 F6:2 Fig. 6. Simulation result of the XTAL oscillator circuit operating at 0.3 V V_{DD} with a reduced Q XTAL resonator.

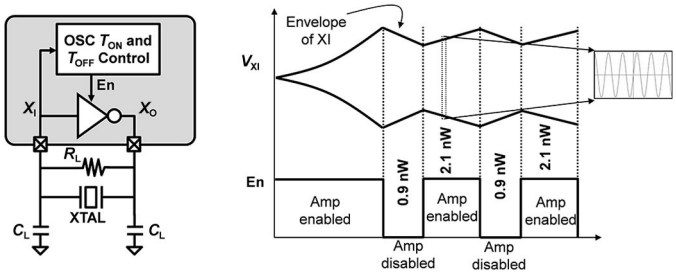
M_N is high, then it will pull down the XO node below REF, which will cause the comparator output to go low. This low signal sets the SAR logic to decrease the drive strength of the transistor M_N. The transistor M_N is realized using series connection of several $0.6\ \mu/10\ \mu$ nMOS as shown in Fig. 4(a). The long transistors are connected in parallel with nMOS calibration switches connected to ground, where only one nMOS switch is on at a time to provide a given drive strength. The SAR logic reduces or increases the drive strength of MN by connecting more or fewer long transistors in series. The size of M_N is successively approximated, and it takes 5 clock cycles. This way M_N can be sized to the right drive strength. Similarly, M_P is sized by setting ENN and ENP to zero and connecting the external resistor to ground. We use an external resistance such that the amplifier can be sized to supply 5–20 nA of bias current, which provides enough drive strength to meet the criteria for oscillation. The calibration is performed at lower V_{DD} of 0.3 V. Fig. 5(a) shows the variation of $\mathrm{R_{NEG}}$ across a 100 point Monte Carlo simulation with and without calibration. The mean R_{NEG} of the amplifier without calibration is -70 kΩ with a 3σ variation of 36 kΩ, whereas the 3σ variation with calibration is $5.4\ k\Omega$. Fig. 5(b) shows the measurement of the amplifier bias current before and after calibration. It varies from 6 to 16 nA across several chips. After calibration, the 3σ variation of the amplifier current was brought down 0.9 nA with a mean of 10 nA. Fig. 6 shows the simulation result of the XTAL oscillator operating at 0.3 V V_{DD} with a power consumption of 2.2 nW. We achieve 2.2 nW power consumption for 30 kΩ XTAL. The power consumption of an XTAL with an ESR of 50 kΩ is going to be 5.6 nW at an R_{NEG} of -100 kΩ and 15 nW for a 90 kΩ XTAL. We use a reduced Q resonator for this simulation to reduce the start-up time and the simulation time. The Q is reduced by lowering the motional inductance and by increasing the motional capacitance of the resonator which has little impact on the required oscillation criteria.

IV. Amplifier Duty Cycling

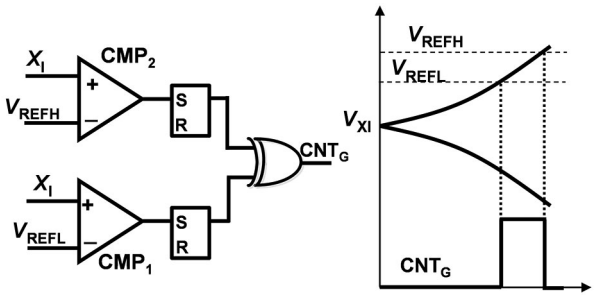
In order for the oscillator to start, $|R_{\mathrm{NEG}}| > \mathrm{ESR}$. The start-up time, the time the oscillator takes to reach the full amplitude, is also controlled by R_{NEG}. The higher the value of R_{NEG}, the faster will be the start-up [12]. However, a higher value of R_{NEG} means higher power consumption. The amplitude of oscillation saturates after start-up. After the oscillation saturates, the R_{NEG} of the amplifier decreases because of the nonlinearity in the circuit due to saturation, and effectively $|R_{\mathrm{NEG}}| = \mathrm{ESR}$ at saturation [11]. The saturation of oscillation creates higher harmonics, resulting in unnecessary power dissipation. While higher power is needed during start-up [12], it is not needed when the oscillation saturates. We propose further improvements in the design to save this power.

The energy of a XTAL oscillator is stored in its equivalent inductor and capacitors. After the saturation of oscillation, the stored energy in the XTAL's equivalent inductor and capacitor is saturated. After the saturation, if the amplifier is disabled, the oscillation will start decaying; and if we enable it again, it will start growing again. The power consumption becomes negligible when the oscillator is disabled. However, oscillation does not die right away and decays slowly, with the time constant given by R_{ESR} and L_m of the XTAL. The output of the XTAL oscillator is still useful and can be used to provide the clock when it is decaying. Therefore, the power consumption of a XTAL oscillator can be further reduced by switching the amplifier. In our design, we switch the amplifier periodically, while keeping the amplitude of oscillation high enough for the clock buffer circuit to detect the oscillation. The work in [15] also proposes a duty-cycling technique to reduce the power consumption of a 39 MHz XTAL oscillator. However, there are several differences between our implementation and the implementation of [15]. It implements a three stage amplifier to reduce the short-circuit current, which is a concern for high frequency oscillators. For low frequency oscillators such as a 32 kHz oscillator operating at 0.3 V V_{DD}, the short circuit current is small. Further, adding three stages of the amplifier in our oscillator will increase the power consumption without duty cycling as each stage will add power overheard. The second main difference between our implementation and [15] is that the control of switches to turn-off the oscillator is external while our implementation is built internally. The authors in [15] obtain the time of decay of oscillation using high-V_T inverters when they stop sensing the oscillations and use this information to turn the oscillator back on again. This implementation can bring the amplitude of oscillation low and cause higher jitter at the output. Also, it uses a fixed time to turn on the oscillator, and the oscillator remains in saturation for more than the required time. Our implementation proposes a method where both TG and TD are proportional to the growth and decay of the oscillation, which we will describe in the following sections. This information is obtained without significantly reducing the amplitude of oscillation. We obtain the correct duty-cycling ratio, and the jitter of our clock is not significantly higher as shown in Fig. 15.

Fig. 7 shows the concept of the control scheme. When the amplifier is disabled, the oscillation at XI will decay with a time constant (TD), which is determined by the R_{ESR} and L_m. When the amplifier is enabled, it grows with a time constant (TG), which is determined by $|R_{\mathrm{NEG}}| - R_{\mathrm{ESR}}$ and L_m [12]. For optimal power savings, the amplifier should be disabled for a time proportional to TD and enabled for a time proportional to TG, as shown in Fig. 7. A counter running on the oscillator output frequency is enabled when the amplitude crosses a



F7:1 Fig. 7. Circuit diagram and operation of oscillator duty cycling.



F8:1 Fig. 8. Circuit to obtain the time constant for the growth of oscillation TG.

set threshold. It counts until CNT_G and stops when the amplitude crosses a higher threshold. This gives us a digital output proportional to TG. Similarly, a CNT_D proportional to TD can be obtained. A clock with the period $(\mathrm{CNT}_G + \mathrm{CNT}_D)$ is obtained, with CNT_G as High and CNT_D as low, as shown in Fig. 7. The proposed technique enables a calibrated switching of the amplifier of the XTAL oscillator and helps in cutting down the power further down to a measured average power of 1.5 nW.

A. Obtaining Time of Growth of Oscillation

Fig. 8 shows the circuit to obtain the TG of the oscillation. It consists of comparators and SR flip-flop. Reference voltages V_{REFH} and V_{REFL} are used for one time calibration to obtain the TG of the oscillator. Threshold voltages $V_{\mathrm{REFH}} = 220$ mV and $V_{\mathrm{REFL}} = 200$ mV are applied at the negative terminal of the comparators, while XI is applied at the positive terminal. Once oscillation amplitude goes above V_{REFL}, the output of CMP_1 goes high, and corresponding SR flip-flop is set. This sets CNT_G to high. A counter is enabled using this signal to count. The amplitude of oscillation keeps on increasing. Once the oscillation crosses V_{REFH}, CMP_2 goes high and sets CNT_G to zero. This stops the counter and sets the value of the counter, which is proportional to the growth of oscillation. The value is digital and is stored, while the time constant circuit is disabled to save power.

B. Obtaining Time of Decay of Oscillation

Fig. 9 shows the circuit implementation for obtaining TD for the oscillator. The circuit is very similar to the circuit used for obtaining TG. It also enables a counter, which counts when XI

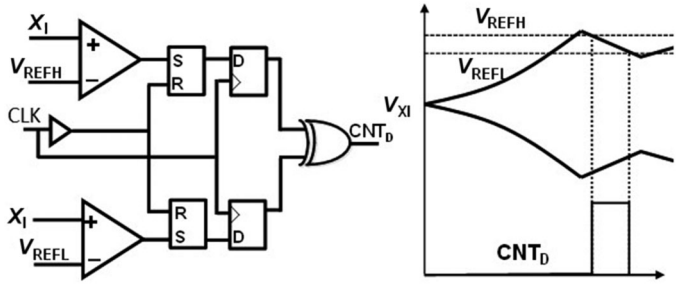


Fig. 9. Circuit to obtain the time constant for the decay of oscillation T_D. F9:1

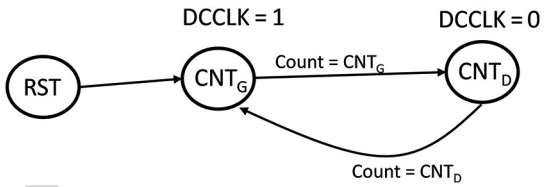


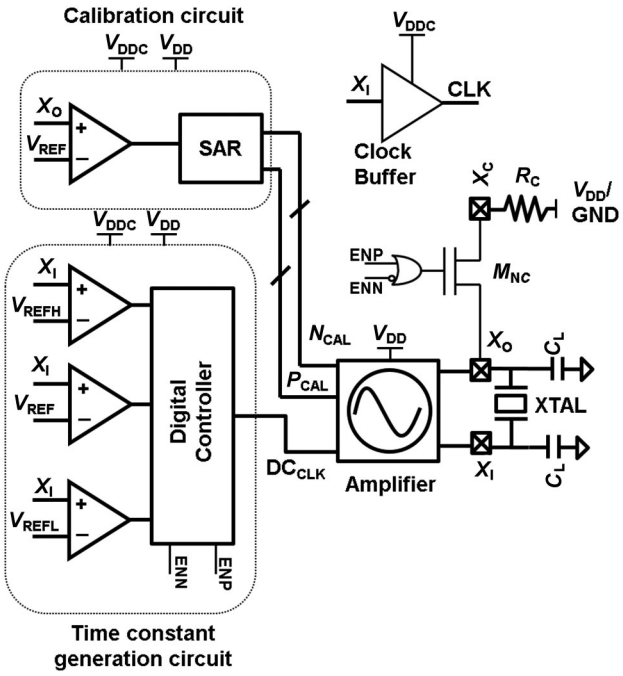
Fig. 10. Digital state machine for generating duty-cycling clock $\mathrm{DC}_{\mathrm{CLK}}$. F10:1

is between V_{REFH} and V_{REFL}. While TG is obtained when the amplifier is enabled, TD is obtained when it is disabled. Both TG and TD are stored digitally, and their corresponding circuits are disabled to save power. After obtaining TG and TD, the oscillator control turns on the amplifier for time = TD and turns it off for time = TG.

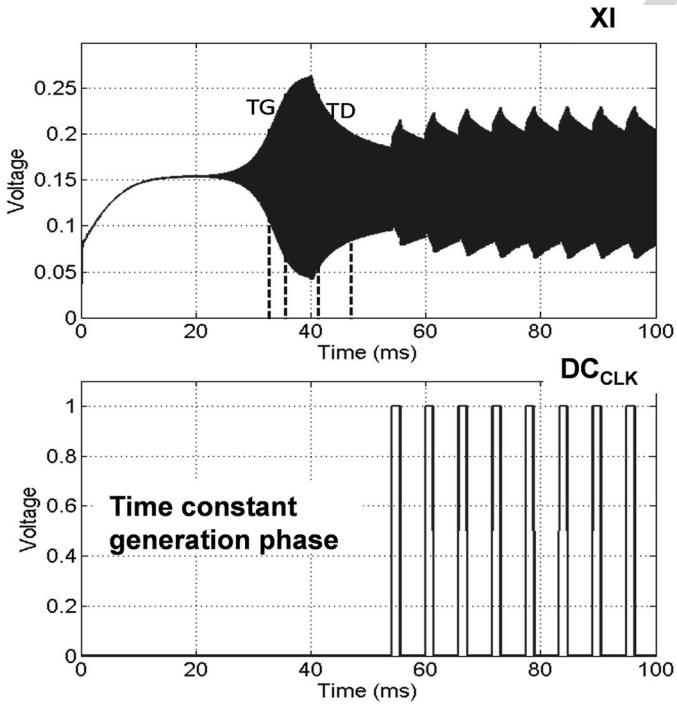
Fig. 10 shows the digital controller for generating the duty-cycling clock $\mathrm{DC}_{\mathrm{CLK}}$ for the oscillator. A counter running on oscillator output frequency is enabled for the duty-cycling mode. It counts for CNT_G and sets $\mathrm{DC}_{\mathrm{CLK}}$ high in that state. It then goes to second state and counts for CNT_D and sets $\mathrm{DC}_{\mathrm{CLK}}$ low for that state. It sets both TG and TD, and a running $\mathrm{DC}_{\mathrm{CLK}}$ is realized.

C. Complete Circuit Architecture

Fig. 11 shows the complete circuit diagram of the proposed XTAL oscillator circuit. First, the calibration of the amplifier is performed, which can be done once after manufacturing. The calibration circuit sets the drive strength of the amplifier and compensates for the process variation. After the calibration, the time constant generation circuit obtains the time of growth (TG) and time of decay (TD) of the oscillator. These time constants are used to configure the clock ($\mathrm{DC}_{\mathrm{CLK}}$) to switch the amplifier on and off. The duty cycle of $\mathrm{DC}_{\mathrm{CLK}}$ is determined by TG and TD with high time = TG and low time = TD. Both the calibration circuit and the time constant generation circuit are operated at higher power supply, V_{DDC} at 0.9 V. The power consumption of the time constant generation and calibration circuit is 4 μW. We perform calibration and time constant generation only once at 0.3 V V_{DD} and at room temperature. Once the $\mathrm{DC}_{\mathrm{CLK}}$ is configured, the time constant generation circuit is powered down. Similarly, the calibration circuit is powered down after calibration and all the digital bits are stored. This eliminates the power overhead of the calibration circuit or time constant generation circuit. The power consumption



F11:1 Fig. 11. Complete circuit architecture of the ULP XTAL oscillator.



F12:1 Fig. 12. Simulation of the duty-cycle XTAL oscillator at 0.3 V V_{DD}.

is given by the amplifier with duty cycling. A clock buffer is used along with a level converter to up-convert the clock to higher voltage if needed. The level converter implements an ULP converter [13] and consumes less than 1 nW for level converting the XTAL output from 300 mV to 0.9 V. Fig. 12 shows the simulation result of the duty-cycling XTAL oscillator. After time constant generation phase, the XTAL operates in the duty-cycling mode, providing a stable clock with a power consumption of 1.5 nW.

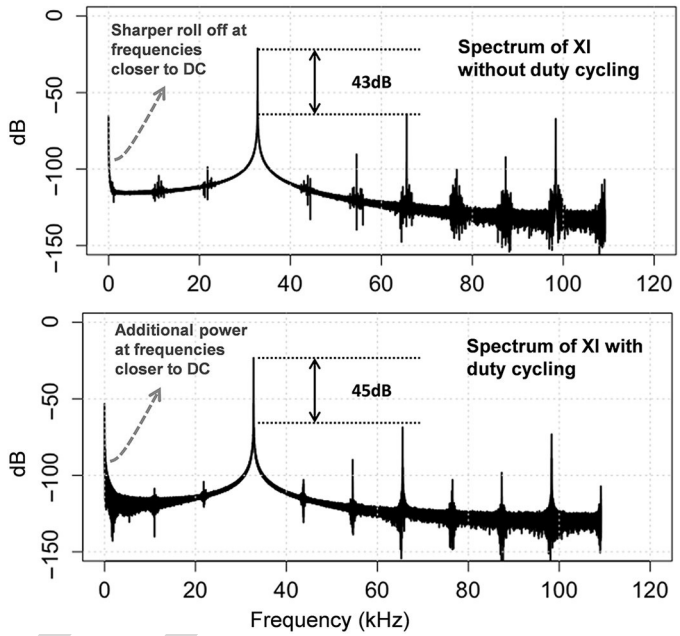
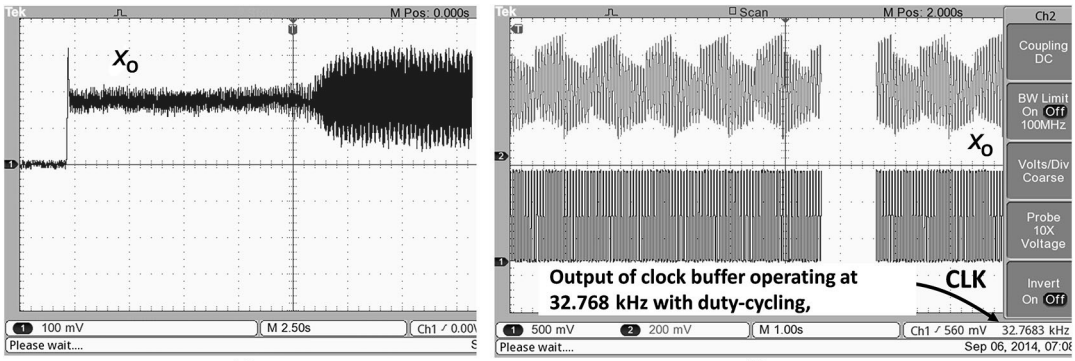


Fig. 13. Spectrum of XI with and without duty cycling. F13:1

The time constants TG and TD are both multiples of the clock period. In our design, the 32.768 kHz clock will be an exact multiple of $\mathrm{DC_{CLK}}$, which is derived from the XTAL output. Further, the high Q of the XTAL makes TG and TD really large, and the frequency of $\mathrm{DC_{CLK}}$ is between 2 and 50 Hz. Fig. 13 shows the spectrum of XI with and without duty cycling. The duty-cycling spectrum shows slightly higher power in frequencies closer to DC. This will result in increase in jitter, which is shown in Fig. 15.

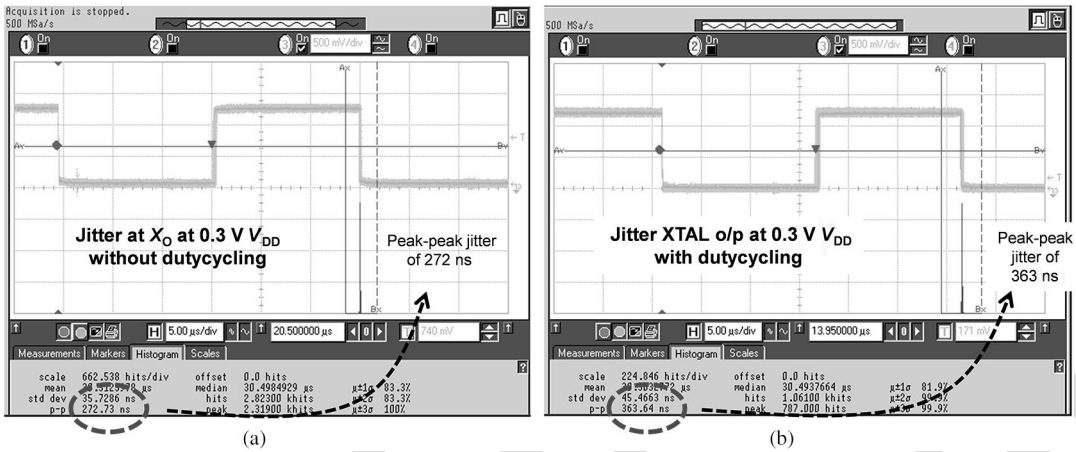
D. Nonlinear Effects

We use small signal analysis to realize the oscillation criteria, where the negative resistance of the amplifier is calculated at the bias condition of the amplifier. The small signal analysis gives the accurate behavior of the oscillator when the amplitude of oscillation is small. However, nonlinearity in the circuit manifests when the amplitude of oscillation starts becoming large. As the amplitude of oscillation increases, the gain of the amplifier decreases as transistors inside the amplifier can no longer stay in saturation. The decrease in the gain will start reducing the effective negative resistance of the amplifier. The higher value of negative resistance over XTAL oscillator's ESR during start-up causes an exponential growth of amplitude. However, as the amplitude increases, the gain of the amplifier drops, causing a decrease in the negative resistance. At saturation, the effective negative resistance (large signal value) of the amplifier becomes equal to the ESR of the XTAL and the circuit reaches steady state condition. Two main concerns are highlighted with respect to using an inverter-based XTAL oscillator in [8]. The first concern is the finite capacitance looking at the output of the power supply used for the inverter-based amplifier. The finite capacitance on the power supply results in the distortion leading to poor frequency stability. Since we use the XTAL oscillator in an energy harvesting application, the power



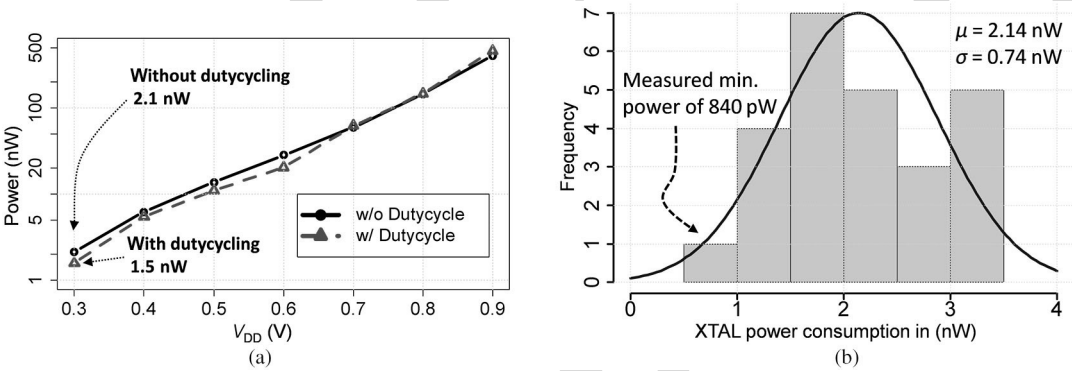
(a) (b)

F14:1 Fig. 14. Measured output waveform of the XTAL oscillator circuit. (a) Start-up of the XTAL oscillator at 0.4 V V_{DD}. (b) Measurement of the waveform at XO
F14:2 with duty-cycling and producing the output clock at 32.768 kHz.



(a) (b)

F15:1 Fig. 15. Measurement of jitter at clock buffer out CLK without duty-cycling and with duty-cycling techniques.



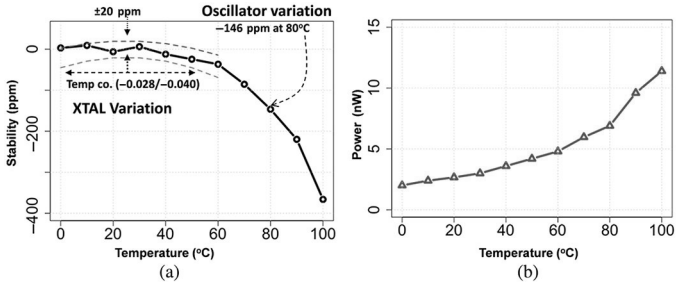
(a) (b)

F16:1 Fig. 16. Measured power consumption of XTAL.

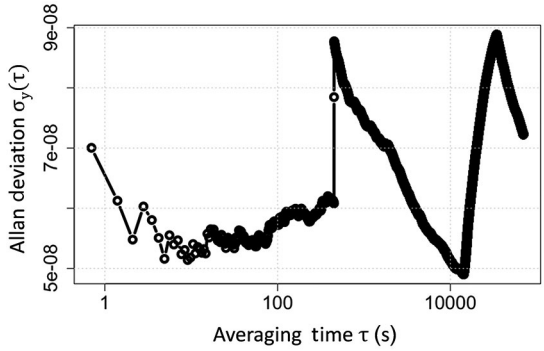
supply will see 100's of µF to few mF of cap at the output. With lower power consumption and large output capacitance on the power supply, we did not see increased instability in the output frequency of the oscillator. The second concern is with respect to power. Authors in [8] point out that higher power in the oscillator results in distortion due large value of gm of the amplifier. This is a concern even with current source-based amplifier. Fig. 13 shows that the power in the second harmonic is roughly 43 dB below the fundamental at 0.3 V V_{DD}. At higher voltage of 0.9 V V_{DD}, we see that second harmonic is roughly 34 dB below the fundamental, resulting in an increase in relative power in harmonics due to higher power. The main advantage of inverter-based oscillator is that the trans-conductance of both nMOS and pMOS are added, which results in overall lower power consumption for the same negative resistance.

V. Measurement Results

The proposed XTAL circuit was implemented in a 130 nm CMOS process. It uses a 3 GΩ external biasing resistor. The XTAL resonator used for this circuit has a Q of 90,000, an ESR of 30 kΩ, and a C_L of 6 pF. The XTAL's performance was

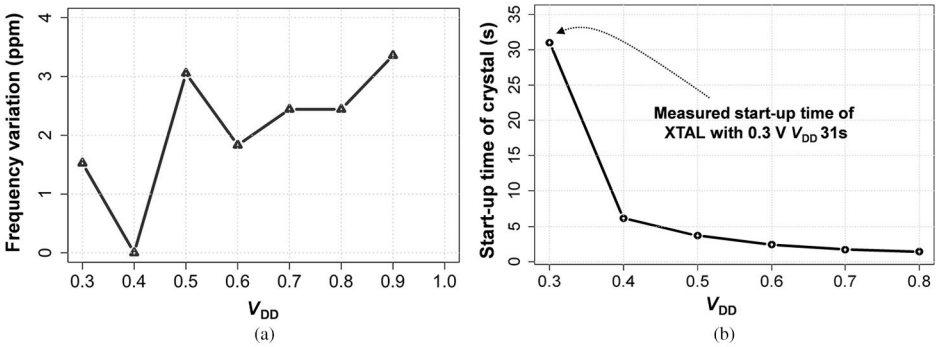


F17:1 Fig. 17. Measured stability and power of the XTAL with temperature, w/o duty
F17:2 cycling, 0.3 V V_{DD} shows stability of 1.87 ppm/°C for a temperature variation
F17:3 of 0 °C–80 °C.

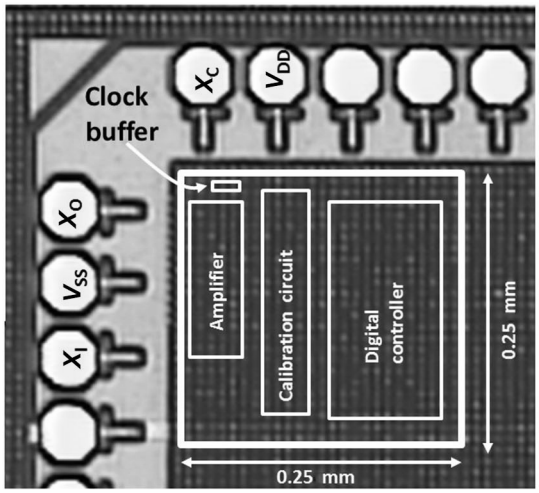


F18:1 Fig. 18. Allan deviation measurement of the XTAL output with duty cycling at
F18:2 0.3 V V_{DD} for approximately 20 h.

measured from V_{DD} of 0.3–0.9 V with a temperature variation from 0 °C to 100 °C. Our measurements were performed with a Keithly power supply with a 2.2 mF capacitance on the supply. Fig. 14(a) shows the measured start-up waveform at XO of the XTAL at 0.4 V V_{DD}. The operation of the XTAL at 0.3 V V_{DD} was measured indirectly by monitoring the clock-buffer output but the waveform at XO cannot be produced at this voltage because of the loading effects from the measurement instruments. Fig. 14(b) shows the measured waveform at XO with duty-cycling technique. The output waveform shows that oscillation is sustained with duty cycling and that the output clock provides a clock with a period of 32.768 kHz. Fig. 15 also shows the measurement of jitter at the output of the clock buffer. The RMS jitter without duty cycling is 272 ns and with duty cycling is 363 ns. Fig. 16(a) shows the power consumption measurement of the XTAL by varying V_{DD}. The measured average power consumption of the XTAL across 25 chips is 2.1 nW without duty cycling and 1.5 nW with duty cycling at room temperature and 0.3 V V_{DD}. The proposed technique does not show significant power improvement at higher V_{DD}. This is because the bias current at higher V_{DD} is much higher than required for oscillation. The output of the oscillator stays well below the full-rail with the duty cycling technique which increases the power consumption because of the short-circuit current in the amplifier as well as in the clock buffer. The overhead of the short-circuit current reduces the benefit of duty cycling at higher V_{DD}. We can save more power, if we configure the oscillator for lower power at higher V_{DD} where duty-cycling technique will show improvement as the short circuit current in the amplifier will decrease. We also configured the XTAL for minimum power consumption required for a sustained oscillation. Fig. 16(b) shows the measured minimum mean power consumption for a sustained oscillation without duty cycling across 25 chips is 2.1 nW with a sigma of 0.71 nW. Measurement for one chip showed a minimum power consumption of 840 pW, where it is approaching the theoretical power consumption limit set by (3) and (4). Fig. 17(a) shows the stability of the oscillator over 0 °C–100 °C at 0.3 V V_{DD}. The chip was calibrated at 0.3 V V_{DD} and room temperature. We maintained this configuration for varying temperature and power supply measurements. Our frequency stability is -146 ppm at 80°C. Fig. 17(a) also shows the variation of the XTAL. Our frequency stability is within the bounds of XTAL variation. The measured frequency stability from 0 °C to 80 °C is 1.85 ppm/°C. The output frequency with duty-cycling technique is 2.5 ppm below the frequency of oscillation without duty cycling at 20 °C. The stability of the overall system is -150 ppm between 0 °C and 80 °C. Fig. 18 shows the measurement of Allan deviation of the XTAL with duty cycling operating at 0.3 V V_{DD}. The measurements were taken with a τ of 0.7 s for approximately 20 h in lab environment. The measurement shows Allan deviation of less than 10^{-7}. Fig. 19(a) shows the variation of the oscillator's frequency with V_{DD}. The power supply variation of our oscillator is less than 7 ppm/V. Fig. 19(b) shows the measured start-up time of the XTAL. The measurement for the start-up time were taken with the oscillator configured for minimum power consumption at 0.3 V V_{DD}. The worst case start-up time is 31 s for 0.3 V V_{DD}. The lower margin on ESR gives higher start-up time. However, our circuit can also start-up in a higher current configuration with all the calibration bits programmed high, which can reduce the start-up time. The circuit can then make use of the lower power configuration. Fig. 20 shows the die photo and the implementation of the XTAL oscillator. The area of XTAL oscillator is $0.0625\ \mathrm{mm}^2$. The Q of the XTAL resonator used for the XTAL oscillator is 90,000, and its ESR is 30 kΩ. We used an external 2 pF load capacitor, which combines with parasitic load capacitance to result in an oscillation frequency of 32.7683 kHz at room temperature. Table I shows the comparison summary of the proposed XTAL circuit with previous work. Our XTAL oscillator circuit consumes 1.5 nW of power and has an area of $0.0625\ \mathrm{mm}^2$. It has over 26% lower power compared to [7] and over 3.7× lower power and 8× lower area compared to [10]. We operated the XTAL circuit at 0.3 V V_{DD}, with a duty-cycling technique. The circuit in [7] uses a self-charging technique to operate the XTAL at 0.15 V V_{DD} to achieve a power consumption of 1.89 nW. The circuit in [10] uses a DLL-based technique and employs two power supplies and two grounds for the amplifier stage. Our circuit uses a single power supply for the amplifier. Previously reported work achieves a power consumption of 22 nW [9] by reducing the amplitude of oscillation. We reduce the amplitude of oscillation by operating the circuit at 0.3 V V_{DD}. The proposed circuit provides a low power, lower area XTAL oscillator circuit. It applies lower voltage design in conjunction with a duty-cycling technique to achieve lower power suitable for ULP devices in IoT networks.



F19:1 Fig. 19. (a) Measured frequency variation with V_{DD}. (b) Measured start-up time of XTAL with V_{DD}.



Parameter	Value
Technology	130 nm bulk CMOS
Total area	250 µm × 250 µm
XTAL's ESR	30 kΩ
XTAL's *Q*-factor	90 000
XTAL's C_m	3.5 fF
XTAL's shunt cap	1.5 pF
C_L	6 pF*
Feedback res. (R_L)	3 GΩ
Calibration res. (R_C)	15 MΩ
XTAL freq. tolerance	± 20 ppm

**The load capacitor includes the parasitic capacitance as well as external capacitance*

F20:1 Fig. 20. Die photo of the XTAL circuit and parameters for the configuration in Fig. 1.

T1:1 TABLE I

T1:2 COMPARISON SUMMARY OF THE DUTY-CYCLED OSCILLATOR WITH PREVIOUS LOW-POWER XTAL

	[7]	[10]	[9]	[14]	This work
Operating frequency	32 kHz	32 kHz	32 kHz	32kHz	32kHz
Area (mm^2)	0.03	0.3	N/A	25	0.0625
Power consumption (nW)	1.89 @0.15V V_{DD} 10 @0.3V V_{DD}	5.58	22	220	1.5 @ 0.3V V_{DD}
Operating V_{DD}(V)	0.15–0.5	0.92–1.8	0.71	3	0.3–0.9
Number of power/Gnd	1/1	2/2	1/1	1/1	1/1
Amplitude of oscillation	N/A	100 mV	65 mV	N/A	230 mV
Temperature stability	–48.8 ppm –20–80°C	–133 ppm –20–80°C	N/A	N/A	–146 ppm (w/o dutycycling) –150 ppm (w dutycycling) 0–80°C
Power supply variation	85 ppm/V	N/A	N/A	2 ppm/V	7 ppm/V
Technology	28 nm	0.18 µm	2 µm	2 µm	0.13 µm

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QUERIES

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