A Design and Theoretical Analysis of a 145mV to 1.2V Single-Ended Level Converter Circuit for Ultra-Low Power Low Voltage ICs

Yu Huang, Aatmesh Shrivastava, Laura E. Barnes and Benton H. Calhoun

Abstract: This paper presents an ultra-low swing level converter with integrated charge pumps that shows measured conversion in a 130nm CMOS test chip from an input at 145mV swing to a 1.2V output. Lowering the input allowable for a single-ended level converter supports energy harvesting systems that need to use very low voltages.

Keywords: Level converter; charge pump; sub-threshold; energy harvesting.

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1. Introduction

Energy autonomy is a critical feature required to enable the large scale deployment of ultra low power (ULP) systems in the internet of things (IoT), with energy harvesting being accepted as a more viable means to provide power. Modern energy harvesting circuits can now harvest energy from input voltages as low as 10mV [2]. However, many challenges face energy harvesting circuits, which require operation at very low power and voltage levels [3]. Figure 1 shows the block diagram of a generic energy harvesting system. The lifetime of the system depends on the energy stored on the energy harvesting capacitor C to provide power for the system. At runtime, as the energy...
stored on C is being consumed, the voltage on the capacitor, $V_{\text{CAP}}$, is decreasing. The voltage at which the system stops operating (system threshold voltage) must be brought down to increase system lifetime. Minimum energy point has been proposed as the most optimal point to operate a system [4]. However, to maximize the utilization of stored energy on a capacitor, the system needs to operate from lowest possible voltage. From the energy utilization perspective, the system threshold voltage should be brought down as low as possible to make full use of the stored energy. To more fully take advantage of the energy stored on the energy harvesting capacitor, SoCs(System on Chip) under ultra-low voltage have been proposed in [5] which operate below 160mV. Typical ULP SoCs frequently use timers to keep the circuit functional even when the voltage is very low [6]. However, the outputs of these ULP sub-threshold circuits also operate at a very low voltage level, which causes communication problems with the core voltage levels off-chip or with other peripheral circuits. Level converters are necessary in such a system to interface between the low voltage domain and the nominal voltage domain. In this paper, we present a low swing level converter that can convert from 100mV (simulation) and 145mV (measurement) level input signals to 1.2V using a single ended charge-pump based topology.

A traditional level converter can convert from nearly 400mV to 1.2V via a cross coupled stage. However, in a low power system, the system life time can be extended by lowering the operation voltage, the same with the energy consumption. Lower input signals can kill the positive feedback and prevent conversion with the traditional design. Several low voltage level converter circuits have been proposed in the literature. A low swing level converter can convert from a range of 210mV to 950mV to 1.2V with a bootstrapping technique [7]. A dynamic logic level converter can convert 300mV to 2.5V, which is employed with a clock synchronizer [8]. However, being a dynamic circuit, it can only operate at higher frequencies and uses higher power and area. A single-ended interconnect circuit achieves level conversion from 300mV [9] but it is dynamic and higher power. In [10], a current-mirror structure is proposed which allows the conversion from 200mV across technologies. A two-stage ULP level converter can convert from 188mV to 1.2V achieving ULP operation [11]. In this work, we present two design constraints for the main stream cross coupled level converter. Also, we propose a level converter that can potentially convert 100mV to 1.2V using a charge-pump. The charge-pump stage increases the swing before level conversion, which helps in initiating the positive feedback. Our measurement results show conversion from 145mV to 1.2V.

This paper is organized as follows: In section 2, we discuss two main categories of conversion techniques for level converter design: amplification-based conversion and boosted swing-based conversion. In this section, we analyze the level conversion techniques in detail and give two design constraints of an amplification-based subthreshold level converter which is the mainstream. In section 3, we propose our own work integrating the two techniques introduced in section 2. We first introduce our design architecture and two different designs based on this architecture. We then show the simulation results of the proposed work. In section 4, we show the chip fabricated using 130nm CMOS technology and the measurement results of the proposed designs. Lastly, we compare our work with the state-of-the-art in section 5.

2. Level Conversion Techniques

In this chapter, we discuss the state-of-the-art level conversion techniques in subthreshold domain. We introduce the level conversion techniques in two categories based on their different fundamental structure and working mechanisms: amplification-based and boosted swing-based level conversions. Specifically, we discuss in detail the theoretical analysis of the amplification-based level conversion.

2.1. Amplification-based Level Conversion

The first main type of level converter design is based on an amplification mechanism which aims to enhance the pull down network. We will analyze this type of design in this subsection.
2.1.1. Designs of amplification-based level converters

Figure 2a and Figure 2b show two of the most traditional amplification-based level converter topologies [12]. Following the naming convention in [10], the level converter shown in 2a is the conventional cross-coupled level converter (CCLC), and the level converter shown in 2b is the current-mirror-based level converter (CMLC). CCLC is a full-swing design which can pull up the input low voltage VDDL up to the high voltage rail VDDH by taking advantage of positive feedback. However, also due to the positive feedback, the conversion capability decreases because it has to meet the ratio constraint between the pull up network and pull down network. CMLC uses a basic current mirror. CMLC has a stronger conversion capability due to the level shift using the differential amplifier action. However, CMLC cannot eliminate the direct current when input is high, which leads to a higher static power consumption.

Figure 2c is a design with an Wilson current mirror (WCMLC) [13]. As discussed in the paper and [10], WCMLC is robust but is not repeatable for the Monte Carlo sizing optimization across different technologies. In [14], they used a three-stage design based on the topology in Figure 2a,
which is able to convert from 200mV to 1.2V. This cascaded design requires three supply voltage and size adjustment for each of the three intermediate conversion stages which increases the design and power management complexity. Based on this work in [14], authors in [11] proposed a two-stage cross coupled level converter as in Figure 3. They added an NMOS header in the first stage to weaken the pull up network (PUN) to enhance the conversion of the shifter. This simplified the design of [14] and achieves the conversion from 188mV in subthreshold. In this paper, we will note this design as a two-stage CCLC (TSCCLC) as in [10].

2.1.2. Theoretical analysis of amplification-based level converters

We will discuss two design constraints here using the example of CCLC: The sufficient conversion condition and balanced switching condition. We will prove the latter gives a stronger design constraint. We will perform all the analysis based on the notation in Figure 4. Finally, we discuss the drawbacks of CMLC.

![Figure 4. Design constraint analysis of CCLC.](image)

**Sufficient conversion condition for CCLC**

The essential point of an subthreshold amplification-based level converter design is to adjust the ratio of the pull up network and pull down network, so that the pull down network is strong enough to achieve the conversion when the input is ‘high’ in subthreshold. As in CCLC, we perform a specific analysis of the design constraints for a sufficient conversion in subthreshold as marked in Figure 4.

In the analysis, we use $V_{in}$ and $V_{tp}$ to represent the threshold voltage for NMOS and PMOS respectively. $k_n$ and $k_p$ are the gain factor of NMOS and PMOS while $k_s n$ and $k_s p$ are for subthreshold. When input switches from ‘low’ to ‘high’, at this moment, $V_1$ is $V_{DDH}$, so $M_1$ works in saturation region:

$$I_1 = k_n(V_{gs} - V_{tn})^2 = k_n(V_{DDL} - V_{in})^2$$

(1)

$I_3$ works in linear region:

$$I_3 = k_p((V_{DDH} - V_2 - V_{tp})(V_{DDH} - V_1) - (V_{DDH} - V_1)^2)$$

(2)

$M_2$ and $M_4$ are off, so we get $I_2$ and $I_4$:

$$I_2 = I_{DP0} \frac{W}{L} e^{\frac{V_{gs}}{nkT}} = k_s p e^{\frac{(V_{DDH} - V_1)}{nkT}}$$

(3)
\[ I_4 = I_{DNO} \frac{W}{L} e^{\frac{k_BT}{nkT}} = k_{sn} \]  \hspace{1cm} (4)

For a successful conversion when input switches from 'low' to 'high', the pull up network should be able to overcome the pull down network at node \( V_2 \) to break the internal equilibrium and trigger the positive feedback:

\[ I_2 \geq I_4 \]  \hspace{1cm} (5)

Represent \( I_2 \) and \( I_4 \) equation 3 and 4:

\[ k_{sp} e^{\frac{q(V_{DDH} - V_1)}{nkT}} \geq k_{sn} \]  \hspace{1cm} (6)

Thus for the minimum scenario:

\[ q \frac{V_{DDH} - V_1}{nkT} = \ln \frac{k_{sn}}{k_{sp}} \]  \hspace{1cm} (7)

Then we get:

\[ V_{DDH} - V_1 = \frac{nkT}{q} \ln \frac{k_{sn}}{k_{sp}} \]  \hspace{1cm} (8)

Assuming that in subthreshold region, the leakage very slowly charges \( C_L \) (on the right part of CCLC), \( V_2 \) will not rise fast and stay close to 0, and \( V_1 \) will stay close to \( V_{DDH} \).

Thus, in equation 2, let \( V_2 = 0 \):

\[ I_3 = k_p (V_{DDH} - V_{tp})(V_{DDH} - V_1) \]  \hspace{1cm} (9)

The sufficient condition for a successful conversion is to break the equilibrium between the pull up network and pull down network and be able to pull down \( V_1 \):

\[ I_1 \geq I_3 \]  \hspace{1cm} (10)

Take in 1 and 9 Thus:

\[ k_n (V_{DDL} - V_{tn})^2 \geq k_p (V_{DDH} - V_{tp})(V_{DDH} - V_1) \]  \hspace{1cm} (11)

Then take 8 into 11, we get the final sufficient condition for a conversion:

\[ \frac{k_n}{k_p} \geq \frac{V_{DDH} - V_{tp}}{(V_{DDL} - V_{tn})^2} \frac{nkT}{q} \ln \frac{k_{sn}}{k_{sp}} \]  \hspace{1cm} (12)

The equation 12 shows that NMOS and PMOS cannot be arbitrarily sized to get the desired ratio for \( k_n \) and \( k_p \), because the sizing of NMOS and PMOS also determines the ratio of \( k_{sn} \) and \( k_{sp} \) at the same time. Therefore, cross coupled level converter (CCLC) cannot be used reliably for subthreshold operations as the subthreshold leakage plays a part in triggering the positive feedback.

**Balanced switching condition for CCLC**

In a level converter design, to get a balance of rising and falling time (i.e., \( t_{LH} = t_{HL} \), we must consider the following constraint:

\[ I_2 = C_L \frac{dV_2}{dt} \]  \hspace{1cm} (13)

And at the same time \( I_2 \) is:

\[ I_2 = k_p (V_{DDH} - V_1 - V_{tp})^2 \]  \hspace{1cm} (14)
Thus, we get:

\[ C_L \frac{dV_2}{dt} = k_p (V_{DDH} - V_1 - V_{tp})^2 \]  \hspace{1cm} (15)

Similarly for \( I_{1L} \), we have:

\[ I_{1L} = k_n (V_{DDL} - V_{tn})^2 - k_p (V_{DDH} - V_1 - V_{tp})^2 \]  \hspace{1cm} (16)

And:

\[ I_{1L} = C_L \frac{dV_1}{dt} \]  \hspace{1cm} (17)

So we get:

\[ C_L \frac{dV_1}{dt} = k_n (V_{DDL} - V_{tn})^2 - k_p (V_{DDH} - V_1 - V_{tp})^2 \]  \hspace{1cm} (18)

Let \( dt = dt \) using 15 and 18:

\[ [k_n (V_{DDL} - V_{tn})^2 - k_p (V_{DDH} - V_1 - V_{tp})^2]dV_2 = k_p (V_{DDH} - V_1 - V_{tp})^2 dV_1 \]  \hspace{1cm} (19)

In a balance design where \( t_{LH} = t_{HL} \), when \( V_1 \) changes from 0 to \( V_{DDH} \), \( V_2 \) changes from \( V_{DDH} \) to 0. Take this into equation 19:

\[ \int_{V_{DDH}}^{0} [k_n (V_{DDL} - V_{tn})^2 - k_p (V_{DDH} - V_2 - V_{tp})^2] dV_2 = \int_{0}^{V_{DDH}} k_p (V_{DDH} - V_1 - V_{tp})^2 dV_1 \]  \hspace{1cm} (20)

Solve the equation 20, we get the design constraint for a subthreshold balanced level converter:

\[ \frac{k_n}{k_p} = \frac{2V_{DDH}(V_{DDH} - V_{tp})}{(V_{DDL} - V_{tn})^2} \]  \hspace{1cm} (21)

The balance design constraint 21 is a much stronger bound than the sufficient conversion constraint 12. In other words, it is more difficult to make a subthreshold level converter with an equal rising and falling time. The bound of 12 gives a design constraint of a successful conversion but cannot guarantee the balance of switching performance.

**Drawback of CMLC**

![Figure 5. Drawback analysis of CMLC.](image)

In the current mirror design (CMLC), the biggest problem is the direct current and the slow conversion in subthreshold. We will do a simple analysis using Figure 5.
When input is ‘high’ ($V_{DDL}$), $M_1$ works in saturation region:

$$I_1 = k_n(V_{gs} - V_{in})^2 = k_n(V_{DDL} - V_{in})^2$$  \hspace{1cm} (22)

But in subthreshold, the case in 22 will be:

$$I_1 = k_n e^{\frac{V_{DDH}}{nkT}}$$  \hspace{1cm} (23)

As the existence of current mirror, we also have:

$$I_1 = C \frac{V_{DDH}}{T_{rise}}$$  \hspace{1cm} (24)

Combine equation 23 and 24:

$$T_{rise} = \frac{C L V_{DDH}}{k_n} \frac{1}{e^{\frac{V_{DDH}}{nkT}}}$$  \hspace{1cm} (25)

From equation 25, a current mirror level converter has a very slow conversion in subthreshold (low VDDL). This is the biggest bottleneck of this kind of design.

### 2.2. Boosted Swing-based Level Conversion

The other type of level converter is the boosted swing-based level converter. Different with amplification-based level converters, boosted swing-based conversions happen by pulling the ‘high’ input signal higher first through boosting techniques. This is usually achieved by taking advantage of the characteristics of a capacitor.

#### 2.2.1. Designs of boosted swing-based level converters

![Figure 6. Boosted swing-based level converter structure](image)

Figure 6 is a design based on bootstrapping effect as reported in [15], lrc-converter as called in [7]. The drivers are enhanced by the bootstrapping techniques through the capacitor $C_b$. In a boosted swing-based level converter like Figure 6, when the input is low, the output is pulled up to VDDH by $M_4$. The left plate of $C_b$ is ‘0’ and the right plate is pulled up to VDDL by $M_0$. When the input is high (VDDL), $M_2$ passes a ‘0’ to $M_0$’s gate and turns it on, while $M_1$ is turned on at the same time.
In this phase, the left plate of $C_b$ is pulled up from 0 to $V_{DDL}$ (in the previous phase) and the right plate is pulled up from $V_{DDL}$ to $2*V_{DDL}$. The boosted $2*V_{DDL}$ is passed to the gate of $M_4$. In order to pull down the output to 0, it has to meet this condition to turn off $M_4$ completely:

$$2 * V_{DDL} > V_{DHH}$$

(26)

If this condition is not met, it will result in static current through $M_4$. This design requires two power supplies: $V_{DHH}$ and $V_{DDL}$ which increases the design complexity. In conclusion, the major problem of this level converter design is that it is dynamic and only works at high frequency. For example in Figure 6, the gate of $M_4$ will slowly decrease to $V_{DDL}$ at lower frequency of signals which causes high static current.

The proposed work in [7] is based on the same bootstrapping effects and reduced the circuit complexity with an improvement of power and delay. A similar design is proposed in [9]. The boosted swing-based design is usually preferred in the interconnect design to work with reducing the power consumption or reboost the signals to communicate with the core chip.

3. Proposed Low voltage Level Converter

In this section, we introduce our proposed low power subthreshold single ended level converter. Our design is based on both the amplification-based and boosted swing-based conversion techniques. The combination of the two design types of level converters achieves a stronger conversion capability that allows a deeper application in subthreshold ICs. This proposed design uses a two-staged architecture: boosting stage and conversion stage. The boosting stage is implemented with a subthreshold charge pump design, while the conversion stage uses the amplification-based techniques.

First, we propose the boosting part: a subthreshold charge pump. Next, we introduce our uniform design architecture which takes advantage of this subthreshold charge pump. According to the architecture, we introduce two level converter designs and show the simulation results accordingly.

3.1. Sub-threshold Charge Pump

![Figure 7. Schematic of the 2X charge pump used in the proposed work.](image-url)
Figure 7 shows the schematic of a 2x charge pump used in the proposed work and its sizing. When \( V_{IN} \) is low, \( M_1 \) turns on which turns on \( M_3 \). \( X \) is pulled up to \( V_{DDL} \) while \( B \) is pulled down to GND by the inverter connected to it. Next, \( V_{IN} \) goes high and turns on \( M_2 \) and \( M_5 \), which leads to the upconversion of \( B \) from 0 to \( V_{DDL} \). Since \( X \) was charged to \( V_{DDL} \) previously, the upconversion of \( B \) causes \( X \) to go from \( V_{DDL} \) to \( 2xV_{DDL} \) at the output of the charge pump. In this design, \( M_4 \) works as a capacitor to implement the boosting.

In deep sub-threshold operation with a VDD between 100mV and 300mV, node \( X \) falls ideally at 200mV and 600mV, respectively. But in sub-threshold, the low slew rate prevents a full doubling of voltage when VDD is very low (<200mV) because of the higher discharge caused by leakage. Thus, we enhanced the pull down network. In this charge pump design, we do not require an additional body bias control circuit.

### 3.2. Implementation of the proposed level converter

We propose two designs that use charge pump outputs to drive a traditional level converter CCLC as in Figure 2a and the improved two-stage amplification-based level converter from [11], as in Figure 3, respectively. We call the former proposed level converter the Charge Pump Boosted Level Converter (CPBLC) in the rest of the paper, and we call the latter proposed level converter the Charge Pump Boosted Ultra Low Swing Level Converter (CPBULS). Following the same naming convention, we use ULS to represent TSCCLC in the following comparison to simplify the relationship between different structures.

#### 3.2.1. Uniform architecture

Figure 8 shows the architecture of the proposed topology, which combines two charge pumps and a level converter design. The first stage provides the differential inputs doubled by the 2x charge pumps. The second stage is a cross-coupled differential inverter (e.g., the level converter designs in 2) that restores the final output to full swing (0 to VDDH). The output of the charge pump stage overpowers the equilibrium of the second stage and drives the PMOS to pull up the internal node (e.g., A or B in Figure 2a) and trigger the positive feedback within the conversion stage.

#### 3.3. CPBLC and CPBULS

Derived from the same proposed architecture, we use the boosting power of the sub-threshold charge pump to trigger the conversion. We will omit the schematic of CPBLC and CPBULS, since their second stages have the same structure of CCLC as in Figure 2a and TSCCLC as in Figure 3.
3.3.1. Simulations

In Figure 9, it shows the functional waveform of CPBULS from simulation of a VDDL of 120mV. In fact, CPBLC works in a similar way. The signals labeled in Figure 9 correspond to the signals in Figure 8. As $V_{IN}$ goes high or goes low, one of the charge pump outputs, e.g. $CP_{OUT}$, increases and thus initiates the positive feedback in the conversion stage, resulting in the amplification-based voltage conversion. From observation, when $V_{IN}$ just reaches its highest value (120mV), the conversion cannot be successfully triggered. Instead, the boosting stage takes in $V_{IN}$ and pull it up to 200mV from 120mV, as shown as $CP_{OUT}$. When $CP_{OUT}$ is boosted to around 200mV, the voltage conversion of the second stage successfully happens. This is as explained in section 2: the boosted $CP_{OUT}$ successfully satisfies the sufficient conversion constraint in 12. In other words, the boosting stage lowers the constraint of a sufficient conversion for the same amplification-based level converter design. Also, in Figure 9, we can see $CP_{OUT}$ will slowly decreases to $V_{DDL}$ too like the design in Figure 6. But the difference is, in our design, this will not cause static current.

![Figure 9. Functional waveform of CPBULS. This figure was originally used in [1]](image)

Figure 10 shows the minimum input swing results of 100 Monte Carlo simulations for CPBULS, CPBLC, and ULS level converters. The charge pump technique decreases the minimum operating voltage of [11] (TSCCLC), further lowered down to an average of 128mV, while the best case (among the 100 iterations) is 99.6mV in CPBULS, and an average of 171mV in CPBLC.

Figure 11 shows the simulation results of the minimum input voltage of CPBULS (red) and CPBLC (blue) level converters under different temperatures. At -20°C, CPBULS and CPBLC can work at 145.4mV and 192.8mV respectively, while at 100°C, they can work at 116.4mV and 144.3mV respectively. Simulation shows that our charge-pump based level converter has lower temperature dependence for minimum operating voltage.
Figure 11. Simulation results of the minimum input voltage vs. temperature of CPBULS and CPBLC level converters. This figure was originally used in [1]

Figure 12. Die photo of the fabricated chip under 130 nm technology. This figure was originally used in [1]

4. Measurements

The proposed design was fabricated in a 130nm CMOS process. Figure 12 shows the die photo of the test chip. The subthreshold charge pump takes 280 $\mu$m$^2$, while CPBLC and CPBULS take around 466 $\mu$m$^2$ with an unoptimized layout design and necessary peripheral circuits.

Figure 13 shows the measurements of the 2x charge pump from 15 chips, which starts working from a 170mV input in the worst case. We show the simulation result together with the measurement results: The blue lines are the measurement results while the red line is from simulation. After $V_{IN}$ is higher than 200mV, the boosting factor is stable at 2x.

Figure 14 shows the measurement results of the minimum operational input swing for CPBULS, CPBLC, and ULS level converters across the 15 chips. The CPBULS can achieve a mean minimum input voltage of 157mV, while the CPBLC achieves the same at 198mV. The CPBULS can reach a lowest input voltage of 145mV. The limitation of this design is slower transition times that lead to higher energy per conversion due to the extra leakage.

Figure 15 shows the energy-delay measurement of CPBLC and CPBULS across 15 fabricated chips. The measurements were taken at three points: 200mV, 300mV, and 500mV. CPBLC and CPBULS can operate with a frequency of 35.6kHz (28us) and 50.1kHz (19.96us) respectively at 200mV for the best case, with a mean value of 12.8kHz and 22.0kHz respectively. The best operation frequency is 66.9kHz and 136.6kHz at 300mV, 109.7kHz and 139.4kHz at 500mV, for CPBLC and CPBULS respectively. As the operation voltage increases, the delay decreases, which is expected in an energy
Figure 13. Simulation and measurement results of the input vs. output voltage of the charge pump stage of the level converter. This figure was originally used in [1].

Figure 14. Measurement results of the minimum input voltage of CPBULS, CPBLC and ULS level converters.

Figure 15. Energy-delay for CPBLC and CPBULS from measurement across 15 chips.

harvesting system where the worst case is when the operation voltage is the lowest. In subthreshold energy harvesting system, there is a lot of voltage variation. The proposed work is designed for an unregulated power supply, which can still successfully work at worst cases (aka, when the operation voltage goes very low). From the measurement results of the 15 chips we fabricated, the best EDP value is 0.0015pJ·ms for CPBLC, and 0.0006pJ·ms for CPBULS.
Another source of variations, the process, can also affect the behavior of this design. As in Figure 7, in sub-threshold, the low slew rate results in that node X cannot be charged to 2 * VDDL due to the discharge caused by leakage. Thus in the slow-fast corner, the discharge will further affect the boosting of X. Vice versa, in the fast-slow corner, the discharge is weakened thus the boosting is enhanced. For the same reason, as in Figure 7, we enhanced the pull down network.

5. Conclusion

This proposed level converter design is based on a subthreshold charge pump design as showed in Figure 7. Due to the charge and discharge time of M4, the capacitor, its performance is not as good as conventional level converter at their operating voltages (300-400 mV). However, this design is a better choice for an ultra low power energy harvesting system where performance is not the first priority but the ability of using stored energy is instead, as discussed in section 1. Thus, we try to take more use of the energy collected in the capacitor in Figure 1. The challenge is, the lower the level converter can operate at, the more energy the system can use to obtain a longer lifetime.

Table 1 compares with prior work, both simulations and chip measurements. This proposed charge pump based level converter CPBULS upconverts reliably from 145mV to 1.2V, which is a wider conversion range. The best energy per conversion is reported as 10fJ in [10] from simulation results with a 90nm technology. This work has a relatively lower maximum operating frequency with the lowest input swing, but achieves 1.2pJ energy per conversion which is 30% less than that in [8] from chip measurement, and a 2x conversion ability. This proposed work can further improve the energy utilization of an ultra low power system such as an energy harvesting system.

| Table 1. Comparison between the proposed work and prior work. |
|-----------------|--------------|---------|---------|---------|---------|
| Minimum VDDL    | 188 mV       | 200 mV  | 400 mV  | 300 mV  | 145 mV  |
| Energy/bit      | -            | 10fJ    | 327fJ   | 1.7pJ   | 1.2pJ   |
| Chip/simulation | Chip         | Sim     | Sim     | Chip    | Chip    |
| Maximum frequency | 17.3MHz      | 10MHz   | 1MHz    | 8MHz    | 8kHz    |
| Area(um²)       | -            | -       | 120.9   | 112000  | 466     |
| Technology      | 130nm        | 90nm    | 180nm   | 130nm   | 130nm   |

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

ULP: Ultra low power.
IoT: Internet of things.
SoC: System on chip.
CCLC: Cross-coupled level converter.
CMLC: Current-mirror-based level converter.
WCMLC: Wilson current mirror level converter.
PUN: Pull up network.
PDN: Pull down network.
TSCCLC/ULS: Two-stage cross coupled level converter.
CPBLC: Charge pump boosted level converter.
CPBULS: Charge pump boosted ultra low swing level converter.

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