A 10mV-Input Boost Converter with Inductor Peak Current Control and Zero Detection for Thermoelectric Energy Harvesting

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***ABSTRACT* — A boost converter for thermoelectric energy harvesting in 130nm CMOS reduces the achievable input voltage by 50% to 10mV, which allows wearable body sensors to continue operation with thermal gradients below 1°C. The design uses a peak inductor current control scheme and duty cycled, offset compensated comparators to maintain high efficiency across a broad range of input and output voltages. The measured efficiency ranges from 53% at V_I=20mV to a peak efficiency of 83% at V_I=300mV.**

I. Introduction

Emerging applications like wearable body sensors often rely on harvested energy from sources with small output voltages [1]. For example, the thermal gradient between skin and air, especially under clothing, may only be a few °C, and the challenge of matching thermal impedances in the harvester packaging may leave thermoelectric generators (TEGs) with <1°C, which results in open circuit TEG outputs less than 30mV. Recent boost converters address this problem by lowering the allowable input voltage (V_I), down to 20mV in [1], and by seeking lower start-up voltages, e.g. with the aid of a mechanical switch [3], RF kickstart [1], or transformer [5]. This paper focuses on the challenge of harvesting from lower V_I. Harvesting from low V_I faces several key challenges; low input power demands ultra-low power circuits for good efficiency, offsets make the small V_I hard to detect and use accurately, mismatch can cause significant variation in the peak inductor current (I_P), and accurate zero detection typically requires high current comparators. Further, the system needs a lower start-up voltage. This paper presents a boost converter capable of harvesting from V_I down to below 10mV at efficiencies that are 7% higher than prior work. A voltage-insensitive constant I_P control circuit, maximum power point (MPP) tracking, an integrated CMOS cold-start circuit from 220mV, and the combination of offset compensation with duty cycled comparators enable these results and give efficiencies from 53% at a 20mV V_I to 83% at higher V_I.

II. Architecture of the Boost Converter

Fig. 1 shows the architecture of the boost converter comprising a MPP tracking circuit, a cold-start circuit, a circuit to generate three phases of timing control, and the conventional High Side (HS) and Low Side (LS) boost converter switches. TEGs provide max power when V_I remains at half the open circuit TEG output voltage, so the MPP circuit stores this value on V_{MPP} at the low pulse of *MPPclk*, which also disables the boost converter. When

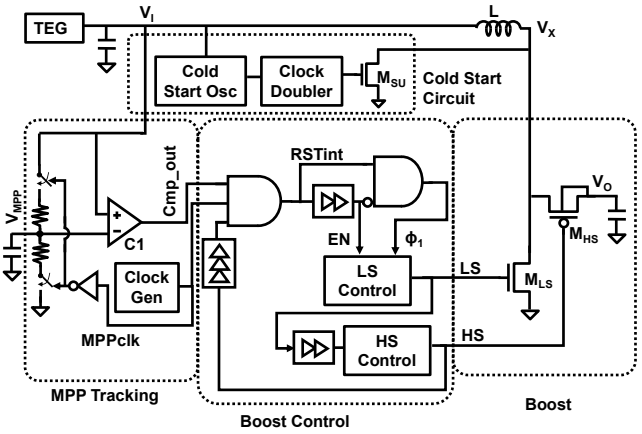

Fig. 1. Architecture of the boost converter with cold start circuit and MPPT circuit.

MPPclk is high, the boost converter operates until $V_I < V_{MPP}$, which disables switching, allowing V_I to recover. Fig. 2 shows the timing of the circuit which implements a pulse frequency modulation (PFM) converter in discontinuous conduction mode (DCM) with the pulse width set to control the peak inductor current (I_P), as described below.

The boost control circuit generates three non-overlapping clock phases, ϕ_1, LS, and HS. The ϕ_1 pulse width is set by a delay line, and this extra phase allows for constant I_P control in the LS timing and offset compensation in comparators throughout the design. The LS pulse width is set to control the I_P, and the HS pulse is controlled to turn off M_{HS} when I_L=0 for zero detection (ZD). Controlling I_P can maximize efficiency across V_I, since it sets the converter at the balance point between larger conduction and switching losses. Conventional approaches (controlling MOSFET's R_{ON}) to set I_P are power intensive and sensitive to mismatch (±20-40% error) [6]. I_P was controlled for a different reason in [2], to achieve zero detection in the following HS phase.

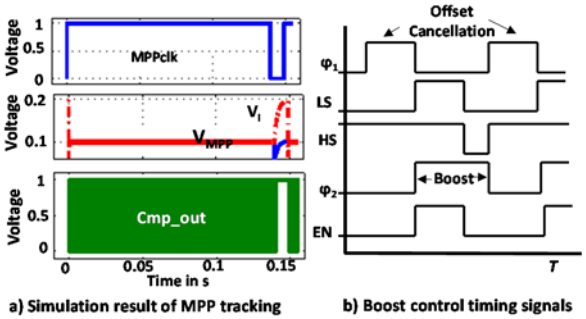

Fig. 2. Timing control of the boost converter includes MPP tracking, offset cancellation in ϕ_1, and boost operation in ϕ_2.

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III. SWITCHING TIMING CONTROL

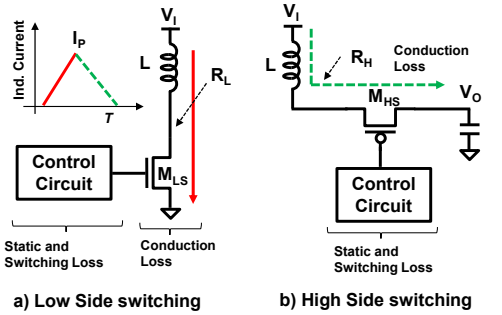


Fig. 3. LS and HS switching operation of the boost converter.

Fig. 3 shows the circuit operation of LS and HS switching in a boost converter operating in DCM. In the LS switching, the inductor current rises from zero to a peak value (I_P), which is discharged onto C_L in the phase HS. The efficiency of the boost converter is limited by the switching loss energy (E_{SW}) for switches and control circuit, static loss (E_{ST}) due to bias currents, and conduction loss (E_{CN}) in the resistance of the switches. The E_{ST} and E_{SW} are generally constants for a given architecture and fixed switch sizes, while the conduction loss depends on I_P. The efficiency depends on I_P as the following analysis describes.

A. *Efficiency Dependence on Peak Inductor Current*

The total energy loss in a boost converter can be given as,

$$E_L = E_{ST}+E_{SW}+E_{CN} \quad (1)$$

E_{CN} has two components, $E_{CN,L}$ and $E_{CN,H}$ for LS and HS conduction loss. For the LS switching, assuming that the switch resistance is small, we can write inductor current as,

$$L\frac{di}{dt} = V_I \quad (2)$$

For LS switching time T_{LS}, the heat loss can be written as, (assuming LS resistance is R_L)

$$E_{CN,L} = \int_0^{T_{LS}} i^2 R_L \, dt \quad (3)$$

Changing (3) to a current integral using (2),

$$E_{CN,L} = \int_0^{I_P} i^2 R_L \frac{L}{V_I} di = \frac{LR_L{I_P}^3}{3V_I} \quad (4)$$

where I_P is the peak inductor current at t=T_{LS}. Similarly, the HS conduction loss is obtained as,

$$E_{CN,H} = \frac{LR_H{I_P}^3}{3(V_O - V_I)} \quad (5)$$

The total conduction loss is given by,

$$E_{CN} = E_{CN,H}+E_{CN,L} = \frac{L}{3}\left(\frac{R_H}{V_O - V_I}+\frac{R_L}{V_I}\right){I_P}^3 \quad (6)$$

Since V_I can be small for this design, R_L should also be small to minimize E_{CN}. Further, for V_O>>V_I, E_{CN} can be given by (4). Since $0.5LI_P^2$ is the energy transferred in each cycle (assuming low losses), the efficiency (η) can be written as,

$$\eta = \frac{E_L}{0.5L{I_P}^2} = \frac{E_{ST}+E_{SW}}{0.5L{I_P}^2}+\frac{R_L I_P}{1.5V_I} \quad (7)$$

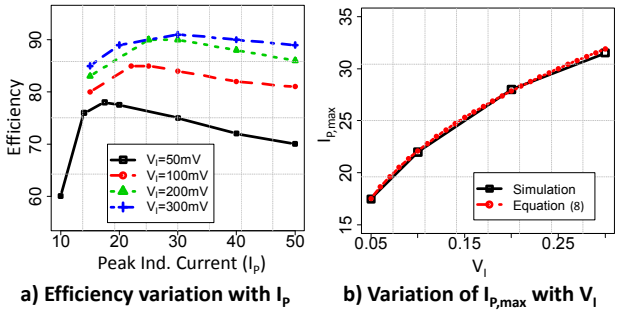


Fig. 4. Simulation of efficiency variation with I_P.

η has a maximum and the corresponding I_P is given by,

$$I_{P,max} = \left[\frac{6(E_{ST}+E_{SW})V_I}{LR_L}\right]^{\frac{1}{3}} \quad (8)$$

Equation (8) also shows that $I_{P,max}$ decreases with V_I. Fig. 4 shows the variation of efficiency with I_P in simulation and with the proposed equation. It shows that at higher values of I_P, η decreases linearly, and at lower values of I_P, it rolls off quickly due to the quadratic dependence shown in (7).

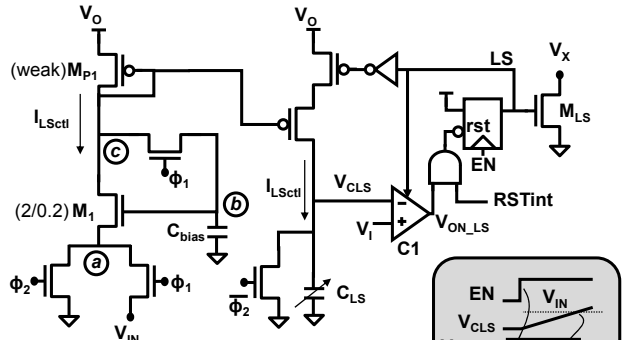
B. *LS Timing Control Circuit for I_P*

Fig. 5 shows the circuit that controls the I_P in LS switching. In the switching phase ϕ_1, node *a* is set to V_I, so nodes *b* and *c* clamp at V_{GS1}=V_I+V_{TM1}. M_{P1} is sized to let M_1 set *c* in ϕ_1 and to keep M_1 in saturation in ϕ_2. During ϕ_2, current in M_1 (long channel) is proportional to $(V_{GS1}-V_{TM1})^2$, which simplifies to $(V_I)^2$. This current, I_{LSctl}, is mirrored and integrated onto C_{LS} until V_{CLS} reaches V_I.

$$I_{LSctl} = C_{LS}\frac{dv}{dt} \rightarrow T_{LS} = C_{LS}\frac{V_I}{I_{LSctl}} = \frac{C_{LS}}{kV_I} \quad (9)$$

where *k* is a constant. Due to the dependence of I_{LSctl} on V_I, the time that LS is on (T_{LS}) is inversely proportional to V_I. Further, assuming negligible drop across M_{LS}, and using (2) which sets I_P, the value of I_P is given by,

$$I_P = \frac{V_I T_{LS}}{L} = \frac{V_I C_{LS}}{kLV_I} = \frac{C_{LS}}{kL} \quad (10)$$



Phase	Node (a)	Node (b)	I_{LSctl}
ϕ_1	V_I	V_I+V_{TM1}	-
ϕ_2	-	V_I+V_{TM1}	α $(V_I+V_{TM1}-V_{TM1})^2$ α $(V_I)^2$

Fig. 5. The Low Side (LS) timing control circuit sets I_P independently from V_I or V_O to maximize efficiency.

I_P has a constant value, $C_{LS}/(k*L)$, independent of V_I and V_O. We select the constant target value of I_P from Fig. 4 based on the anticipated TEG output voltage. However, the value of I_P should decrease with V_I given by (8). In our proposed circuit, I_P does decrease with V_I due to the small voltage drop across M_{LS} which we ignored initially to derive (2). This dependence is not the dependence required by (8). However, it does help to increase efficiency at lower values of V_I. The offset cancellation (not shown) of comparator C1 in phase ϕ_1 enables charging at voltages measured down to 10mV. When the comparator detects that $V_{CLS}>V_I$, it turns off the LS pulse. This circuit consumes no static power since the comparator is on only during times of high power transfer and high I_L, making its power a component of the switching loss. Measurement of I_P control (Fig. 6) shows that it is within 15% of the value proposed by (8) at V_I=50mV and <1% at V_I=150mV or higher. The variation across process (k parameter) is addressed by digitally tuning C_{LS}. C_{LS} can also be tuned for lower V_I operation to improve efficiency.

C. HS Timing Control for Zero Detection

Turning off the HS switch at the I_L=0 point (ZD) is important for efficient operation. Comparator based schemes have been considered too high power for low V_I boost converters, so [2][3] detect V_X after M_{HS} turns off and use its behavior to correct timing for the next cycle. This paper proposes that a comparator based scheme is ideal for micro-power converters if the offset can be very low (~1mV) and the performance is high without costing too much power. Fig. 7 shows a design with these features. Comparator C2 detects I_L=0 by comparing V_X and V_O and immediately turns off M_{HS}. The comparator itself uses a common gate topology (Fig. 7) that is turned on only during the HS and ϕ_1 pulses. Since I_L (and power transfer) is large over most of that time,

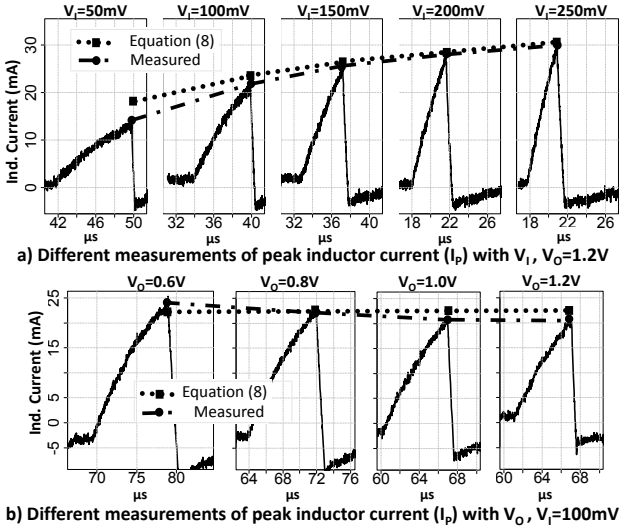


Fig. 6. Measurement results of peak inductor current a) variation with V_I and b) variation with V_O shows that the LS control circuit tracks I_P based on (8) for maximum efficiency.

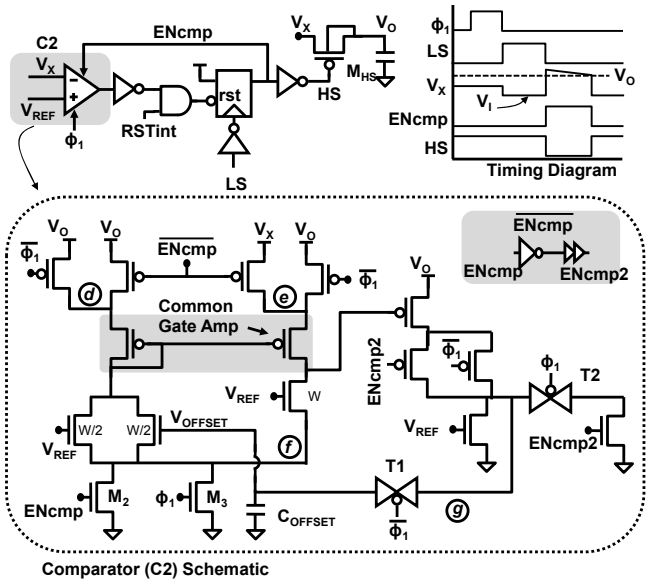


Fig. 7. High Side (HS) timing circuit with an offset-compensated (for offset <1mV) and duty cycled (for low power) comparator.

the extra "switching loss" from comparator-C2 reduces efficiency by only 4% at V_I=20mV and 0.4% at V_I=0.3V, but its high on-current (~10μA) gives a fast response. Offset is never good, but offset can be even more problematic for converters working from low V_I. Phase ϕ_1 provides for offset compensation in the HS comparator. In ϕ_1, nodes *d* and *e* are set at V_O while *f* is set at V_{SS}, and switch T1 is turned on while T2 is off. The feedback from node *g* sets V_{OFFSET} to remove offset in the comparator. If there is no offset in the design, $V_{OFFSET}=V_{REF}$. The measured comparator offset after compensation was <1mV. The other comparators in the converter use a similar offset compensation circuit.

IV. COLD-START CIRCUIT

Fig. 8 shows the cold-start circuit for the boost converter. It consists of a ring oscillator (RO) and a clock doubler circuit. When V_O is below 550mV, POR is low which enables the RO on V_I. The RO can oscillate for V_I>200mV and generates non-overlapping signals p_1 and p_2. Signals p_1 and p_2 go to the clock doubler circuit, which generates LS_SU. The clock doubler circuit uses p_1 and p_2 and implements a 2x charge-pump based clock source to produce a 0 to $2V_I$ swing signal at LS_SU. The increased swing

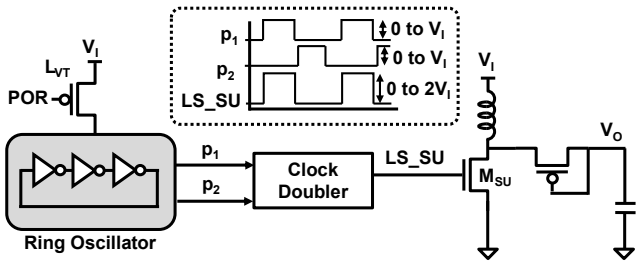


Fig. 8. Cold-start circuit for 220mV startup using clock doubler.

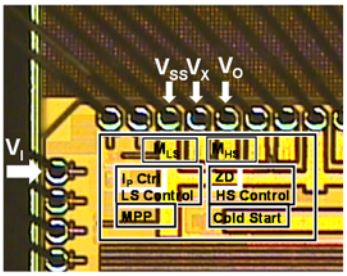
is used for inductor switching to charge V_O. The cold-start circuit is disabled when V_O crosses the POR threshold.

V. Measurement Results

The chip was fabricated in 130nm bulk CMOS (Fig. 9), and the boost converter uses 0.12mm^2. The LS resistance, which is critical for efficiency at low voltages, has a designed value of 0.3Ω. Fig. 6 shows measurements of correct I_P control across V_I and V_O. Fig. 10(a) and Fig. 10(b) show the measurement of Vx at inductor current zero crossing. Node Vx doesn't have overshoots or undershoots at the zero crossing, which indicates near-ideal zero detection using our offset compensated ZD comparator. Fig. 10(c) shows measurement of boost converter operation at V_I=10mV (1mA i/p current). Fig. 11(a) shows the measurement of boost converter operation from cold-start. In this measurement, V_I was set at 250mV for cold-start. After the cold-start, V_I is slowly decreased to 20mV. The measurement shows operation at 20mV. The minimum cold-start voltage was measured at 220mV and the minimum measured operating V_I is <10mV. Fig. 11(b) shows that the efficiency ranges from 21% at V_I=10mV and V_O=0.6V to a max of 83% at V_I=0.3V and V_O=1.1V. We also measured the boost converter operation with a TEG (Laird 430857-500) at the minimum open circuit voltage of 20mV. Table 1 compares this converter to prior works.

VI. Conclusion

A thermoelectric boost converter combines an I_P control scheme with offset compensation and duty cycled comparators to enable energy harvesting from TEG inputs as low as 10mV, 50% lower than prior work. Controlling the I_P allows the converter to sustain high efficiency across a broad V_I range, achieving 53% and 83% efficiency at 20mV and 300mV, respectively, which improves on prior designs. A cold-start circuit enables operation from 220mV, 110mV lower than previous work [4] for start-up without external excitation such as mechanical [3] or RF [1] or use of transformers [5]. These features allow the converter to extend the operating window for thermal harvesting with low thermal gradients, which is ideal for body worn sensors.



Resistance breakdown of LS

Parameter	Value
Technology	130nm bulk CMOS
Total area	600 µm x 200 µm
Inductor value	L=10 µH
V_{IN}-to-V_{SS} LS resistance	300 mΩ (Target)
Inductor DCR	70 mΩ
Bondwire	50 mΩ (1mm,1mil,gold)
NMOS Res	120 mΩ
Layout parasitic	60 mΩ

Fig. 9. Implementation of the boost converter.

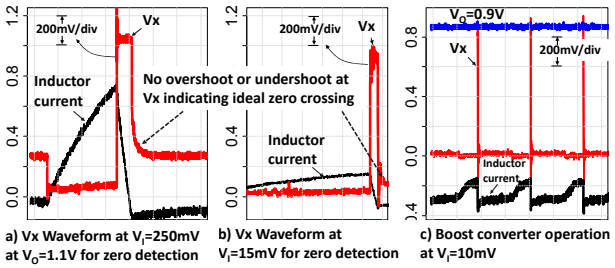


Fig. 10. Inductor switching waveforms a) Vx at V_I=250mV and b) V_I=15mV showing near ideal zero crossing. c) switching operation at 10mV.

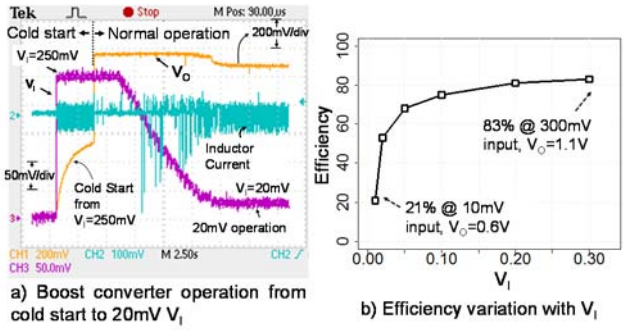


Fig. 11. a) Boost converter cold-starts from 250mV, normal operation from 250mV to 20mV V_I b) Measured efficiency of the boost converter with V_I.

Table 1. Comparison with state-of-the-art energy harvester circuits

	This Work	[2]	[3]	[4]	[5]
Harvesting	TEG	TEG	TEG	Solar / TEG	TEG
Min. V_I	10 mV	20 mV	25 mV	-	40 mV
Cold-Start V_I Voltage	220 mV	600 mV	35 mV w/ mech. kick	330 mV / 5 µW	40 mV w/ X-former
I_{DDQ}	300 nW	~ 1 µW	-	~330 nA	-
I_P Control	✓	×	×	-	×
MPPT	✓	×	✓	✓	✓
η (@ V_I)	83% @ 0.3V	75% @ 0.1V	58% @ 0.1V	80% @ 0.5V, Solar	61% @ 0.3V
η at low V_I	53 % @ 20 mV	46% @ 20 mV	-	-	30% @ 50 mV
Technology	130 nm	130 nm	350 nm	-	130 nm

Acknowledgments

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