

### 21.3 A 6.45 $\mu$ W Self-Powered IoT SoC with Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios

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A 1 trillion node internet of things (IoT) will require sensing platforms that support numerous applications using power harvesting to avoid the cost and scalability challenge of battery replacement in such large numbers. Previous SoCs achieve good integration and even energy harvesting [1][2][3], but they limit supported applications, need higher end-to-end harvesting efficiency, and require duty-cycling for RF communication. This paper demonstrates a highly integrated, flexible SoC platform that supports multiple sensing modalities, extracts information from data flexibly across applications, harvests and delivers power efficiently, and communicates wirelessly.

The SoC (Fig. 21.3.1) integrates a power management unit (PMU) with a boost converter for solar and thermoelectric generator (TEG) energy harvesting and a single-inductor, multiple-output (SIMO) DC-DC converter for high end-to-end self-powered efficiency. An asymmetric radio leverages ultra-low power (ULP) ultra-wideband (UWB) transmission and an always-on ULP receiver to reduce RF power significantly relative to prior SoCs for communication at higher data rates in an energy harvesting platform. The sensing interface includes a 4-channel (2 $\mu$ W/channel) analog front-end (AFE) [2] and SPI with variable voltage output pads (0.4-to-3.3V) for commercial sensor compatibility. The OpenMSP430 (OMSP) processor and a suite of accelerators can execute numerous biomedical and environmental signal processing algorithms (e.g. filtering, peak detection, histograms) combining ASIC energy efficiency and flexibility. A lightweight control unit (LCU) can manage chip data and node control while the OMSP is off, and uses a custom ISA and interrupt-driven programs to reduce the program size. The chip's flexible clocking unit, containing a programmable ADPLL and configurable system clock, can drive the system clock from a low-power crystal. The digital blocks run in sub-threshold on a 0.5V supply from the PMU, while the radios use both the 1.2V and 0.5V rails.

The chip uses two independent buses (Fig. 21.3.1) controlled by either the OMSP or LCU (for bus 1) or by the two-channel DMA (bus 2). The LCU can configure the OMSP as the main controller or as a bus peripheral that is used only for ALU or background operations. Since most data transfer occurs between the peripherals and the on-chip memories, the two-channel DMA (configured by OMSP or LCU) allows data movement on bus 2 in parallel with chip control on bus 1. Peripheral block wrappers decode and route bus data and manage independent block reset, clock gating, power-gating, and power mode settings. Most peripherals contain three power domains: always-on configuration registers, a bus decoder domain, and a block core logic domain (Fig. 21.3.2). Programmable peripherals include a 4-channel, programmable FIR filter, a CORDIC, 16-point complex FFT/IFFT, two timer modules with capture/compare, a multiplier, and heart rate (R-R) AFIB detection. This suite of hardware accelerators supports flexible processing for a wide range of applications.

An on-chip 187.5kHz to 500kHz ADPLL uses a dual-loop architecture that eliminates the divider to consume 300-600nW from 0.5V with jitter <0.1% in 0.07mm<sup>2</sup>. The entire ADPLL was implemented using standard digital design flows and automatic place and route (APR). An integrated crystal oscillator (31.25 kHz) gives the reference to the ADPLL, and a digital clock module lets the LCU or the OMSP control the clock frequency and reset state for the SoC. The SoC has a 4kB data memory and three, 2kB memories: Tx buffer, LCU instruction memory, and OMSP instruction memory. All SRAMs use an 8T sub-threshold bitcell and a read before write scheme. The memories are partitioned into 1KB, independently power gate-able banks and operate down to 0.35V.

The integrated energy harvesting and PMU couples a boost converter and SIMO DC-DC converter to achieve a measured 74.9% end-to-end (boost and DC-DC) peak efficiency for the 1.2V output (65.7% end-to-end efficiency for the 0.5V output) for a 100 $\mu$ A load while harvesting from indoor solar at the maximum power point (MPP) input voltage of 1.3V. Figure 21.3.3 shows the complete powertrain architecture. The system can harvest energy from a photovoltaic cell (PV) (e.g., with an open circuit voltage of 1.7V) or from a TEG. The boost converter [4] can harvest energy from a  $V_{IN}$  as low as 10mV and charges  $V_{CAP}$  to up to 1.4V. An integrated MPP tracking (MPPT) circuit tunes the input impedance of the boost converter to extract the maximum energy from the ambient source (either the TEG or PV). A SIMO DC-DC converter regulates  $V_{CAP}$  to a 1.2V and 0.5V supply to improve end-to-end efficiency over [2], which used on-chip LDOs. Figure 21.3.3 shows the measurement waveforms for the PV power in the presence of indoor light, the MPPT operation, and the regulated 1.2V and 0.5V outputs at a load current of 100 $\mu$ A. Figure 21.3.3 also shows the end-to-end efficiency vs. input voltage for both output rails. The system achieves peak end-to-end efficiency at the MPP of the solar cell, which is measured to be 1.3V. An integrated digital power-management unit (DPM) checks the available energy on the capacitor before allowing system operations, and performs system mode changes or shutdown if available energy is low by overriding the block level power mode configuration.

Despite the frequent use of heavily duty-cycled radios in low-power applications, maintaining high data-rate RF communication is needed in many IoT applications. To support this, we use an asymmetric RF architecture to minimize power on node (Fig. 21.3.4). The UWB transmitter uses OOK modulation with a data rate of 187.5kbps and a center frequency of 3.99GHz with a 500MHz bandwidth. It consists of a pulse-width generation circuit that uses two separate signal paths with different variable delays to create a short pulse, which is then used to enable/disable a ring oscillator, creating the UWB pulses. A Class AB power amplifier buffers the signal onto the antenna. The Tx FSM has a 2kB sub-threshold memory buffer that stores the raw data as well as any synchronization and preamble headers the base station receiver might need. The Tx FSM clocks the data out of the memory and serializes it before transmission, and the FSM can append a timestamp to the serial data as needed. The CDMA wakeup receiver (WuRx) [5] has four separate interrupt outputs, one hardcoded to each of the OMSP and LCU, and two other programmable outputs. Each interrupt is triggered by a unique 15-bit OOK modulated Kasami code. The WuRx can also be used to receive data packets at 8kb/s.

The chip was tested end-to-end for motion capture with an ADXL362Z accelerometer (over SPI) while powered from indoor solar by the PMU. The chip consumes 6.45 $\mu$ W while streaming raw motion data wirelessly over UWB. Figure 21.3.5 shows the flexible data path capabilities of the SoC for motion capture applications and transmission of accelerometer data using the on-chip SPI with variable voltage pads. Figure 21.3.6 compares the SoC (Fig. 21.3.7) to prior work. To date, this work has the highest level of integration, including energy harvesting and a full transceiver, for the lowest power. This work also has the highest energy harvesting / regulation efficiency, and achieves lower RF connectivity power by 38x. The carefully integrated ULP components on this SoC support numerous IoT applications on a self-powered platform.

#### Acknowledgements:

This work was funded in part by ONR, by NSF (1035771), and by the NSF NERC ASSIST Center (EEC-1160483).

#### References:

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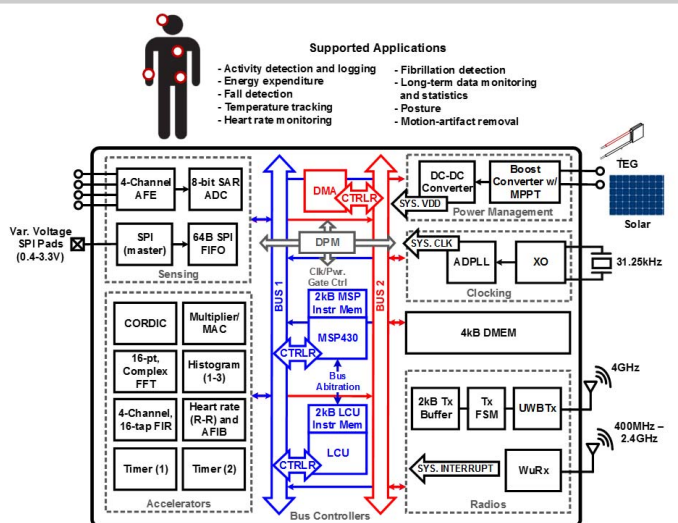


Figure 21.3.1: System block diagram for the SoC, highlighting supported applications and interfaces.

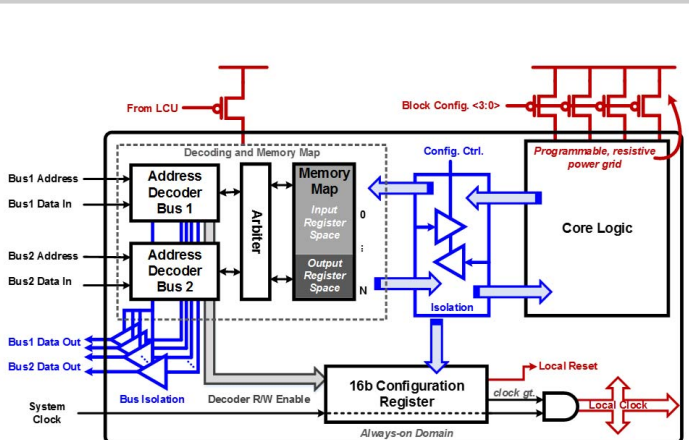


Figure 21.3.2: Block-level architecture of the peripheral units showing fine-grained clock and power gating.

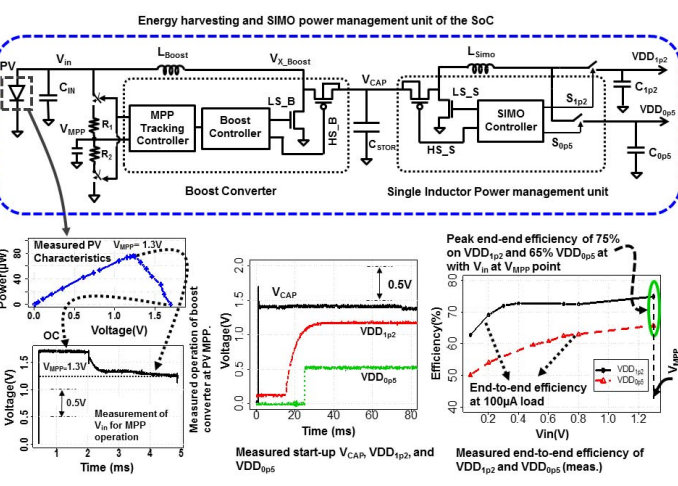


Figure 21.3.3: Circuit architecture and measurement of the energy harvesting and power management unit of the SoC.

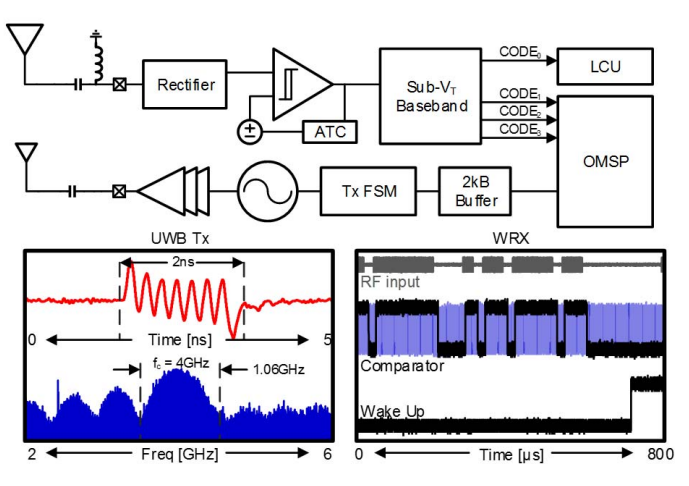


Figure 21.3.4: Transceiver architecture and performance.

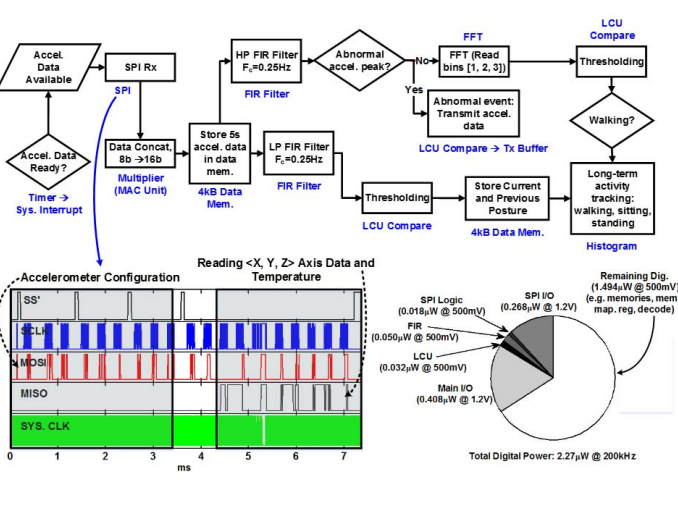


Figure 21.3.5: Supported system demo block diagram and power breakdown using the digital SPI interface and ADXL362Z accelerometer.

	This Work	ISSCC '14 [1]	JSSC '13 [2]	ISSCC '14 [3]
Sensor Interfaces	Analog (ECG, EEG, EMG), Digital (SPI, I2C, UART)	Analog (ECG, bio-impedance), Digital (SPI, I2C, UART)	Analog (ECG, EMG, EEG)	Analog (ECG)
MCU	MSP430	ARM Cortex M0	8-bit PIC	ARM Cortex M0
Peripherals	DMA, FIR, FFT, CORDIC, Timer, Histogram, Multiplier, R-R AFIB	DMA, Matrix-Multiply-Accumulate	DMA FIFO, FIR, Envelope Detector, R-R AFIB	FIR, FFT
On-Chip Memory	12 kB (0.35 V - 0.7 V)	128 kB	5.5 kB	3.7 kB
DVS	Y	N	Y	N
Digital Power Management	Y	N	Y	N
Flexible Clocking	ADPLL (187.5 to 500 kHz with 1/2/4/8)	MCU Clock (1-20 MHz)	200 kHz (with 1/2/4)	10 kHz
Digital Power (Active)	2.27 $\mu$ W	120 $\mu$ W	2.1 $\mu$ W	45 nW
Integrated PMU	Y	N	Y	N
Energy Harvesting	solar, TEG	-	TEG	-
End-End PMU Efficiency	74.9%	-	38%	-
Regulated Output Voltages	1.2 V, 0.5 V, Variable	-	1.2 V, 1.0 V, 0.5 V (2)	-
SIMO Regulation	Y	N	N	-
Boost Voltage	10 mV	-	30 mV	-
ADC Resolution	8	10	8	8
ADC Sampling Frequency	128/256 Hz	500 Hz	128/256 Hz	500 Hz
AFE Channels	4	3	4	1
Integrated Transceiver	Y	N	N	N
Tx Band	2400 MHz - 2480 MHz (3.99 GHz center)	-	402 / 433 MHz	-
Tx Data Rate	187.5 kbps	-	200 kbps	-
Tx Output Power	-28.9 dBm	-	-18.5 dBm	-
Tx Power	4.18 $\mu$ W	-	160 $\mu$ W	-
Rx Center Frequency	400-2400 MHz	-	-	-
Rx Data Rate	7.8125 kbps	-	-	-
Rx Power	112 nW	-	-	-
Rx Energy/15-bit/Wake-Up	161 pJ/bit	-	-	-
Technology	130 nm	180 nm	130nm	65 nm
Die Area	13.49 mm <sup>2</sup>	49.00 mm <sup>2</sup>	8.25 mm <sup>2</sup>	3.32 mm <sup>2</sup>
Max. Voltage	1.4 V	1.2 V	1.2 V	0.6 V

Figure 21.3.6: System comparison table.

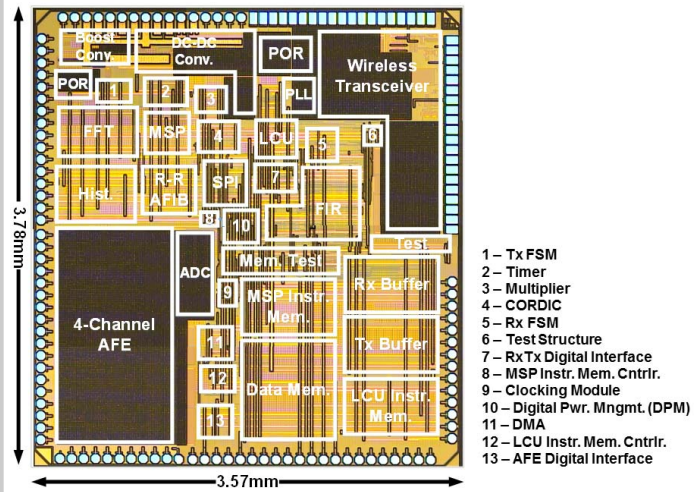


Figure 21.3.7: Chip micrograph.